Single-/Dual-Supply, High Voltage Isolated IGBT Gate Driver with Miller Clamp

Preliminary Technical Data

ADuM4135

FEATURES

- 4 A peak drive output capability
- Output power device resistance: <1 Ω
- Desaturation protection
  - Isolated desaturation fault reporting
  - Soft shutdown on fault
- Miller clamp output with gate sense input
- Isolated fault and ready functions
- Low propagation delay: 50 ns typical
- Minimum pulse width: 50 ns
- Operating temperature range: −40°C to +125°C)
- Output voltage range to 30 V
- Output and input undervoltage lockout (UVLO)
- Creepage distance available: >8 mm
- 50 year lifetime for 500 V rms or 1200 V dc working voltage
- Safety and regulatory approvals (pending)
  - UL recognition
    - 5 kV_{AC} for 1 minute per UL 1577
  - VDE certificate of conformity
    - VDE-0884-10 (reinforced)
    - DIN60747-5-2 (VDE0884 Part 2)/2003 (basic)

APPLICATIONS

- MOSFET/IGBT gate drivers
- PV inverters
- Motor drives
- Power supplies

GENERAL DESCRIPTION

The ADuM4135 is a single channel gate driver specifically optimized for driving insulated gate bipolar transistor (IGBTs). Analog Devices, Inc., iCoupler® technology provides isolation between the input signal and the output gate drive.

The ADuM4135 provides a Miller clamp to provide robust IGBT turn-off with a single rail supply when the gate voltage drops below 2 V. Operation with unipolar or bipolar secondary supplies is possible, with or without the miller clamp operation.

The Analog Devices chip-scale transformers also provide isolated communication of control information between the high voltage and low voltage domains of the chip. Information on the status of the chip can be read back from dedicated outputs. Control of resetting the device after a fault on the secondary is performed on the primary side of the device.

Integrated onto the ADuM4135 is a desaturation detection circuit that provides protection against high voltage short-circuit IGBT operation. The desaturation protection contains noise reducing features such as a 300 ns masking time after switching event to mask voltage spikes due to initial turn-on. An internal 500 µA current source allows for low part count, but the internal blanking switch allows for the addition of an external current source in case more noise immunity is needed.

The secondary UVLO is set to 11 V with common IGBT threshold levels in mind.

FUNCTIONAL BLOCK DIAGRAM

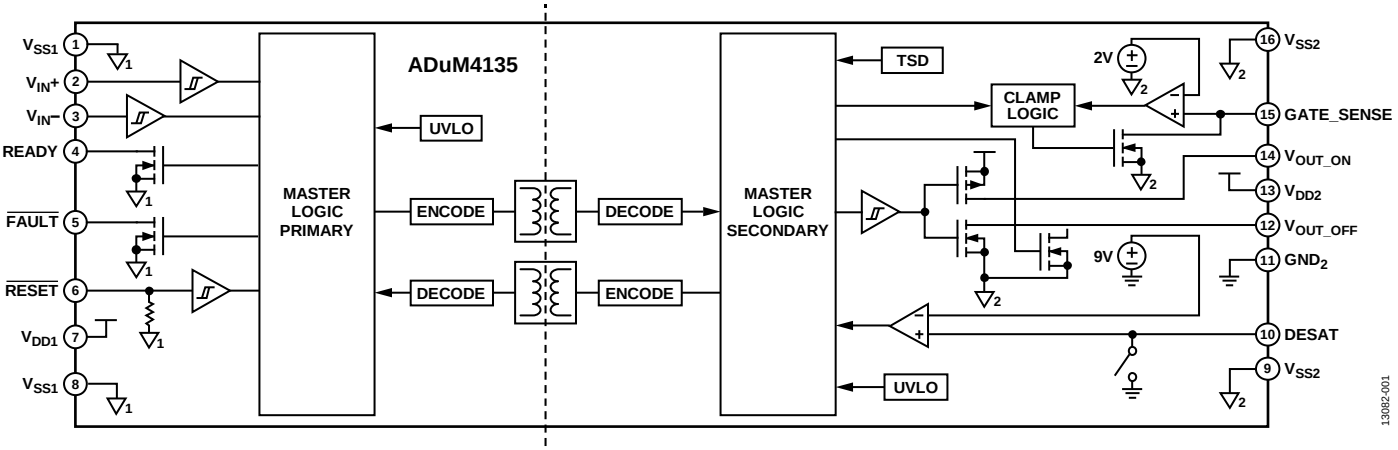

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

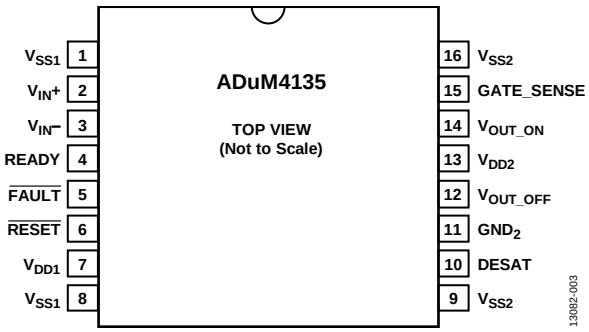

Figure 2. Pin Configuration

Table 1. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{SS1}	Ground Reference for Primary Side.
2	V_{I+}	Positive Logic CMOS Input Drive Signal.
3	V_{I-}	Negative Logic CMOS Input Drive Signal.
4	READY	Open-Drain Logic Output. Connect this pin to a pull-up resistor to read the signal. High state shows device is functional and ready to operate as gate driver. Presence of READY low precludes gate drive output from going high.
5	$\overline{\text{FAULT}}$	Open-Drain Logic Output. Connect this pin to a pull-up resistor to read signal. Low state when desaturation fault has occurred. Presence of fault condition precludes gate drive output from going high.
6	$\overline{\text{RESET}}$	CMOS Input. When fault exists, bring low to clear fault.
7	V_{DD1}	Input Supply Voltage on Primary Side, 2.3 V to 5.5 V Referenced to V_{SS1}.
8	V_{SS1}	Ground Reference for Primary Side.
9	V_{SS2}	Negative Supply for Secondary Side, −15 V to 0 V Referenced to GND_2.
10	DESAT	Detection of Desaturation Condition. Connect this pin to an external current source or a pull-up resistor. This pin can allow for NTC temperature detection or other fault conditions. A fault on this pin asserts a fault on $\overline{\text{FAULT}}$ on the primary side. Until the fault is cleared on the primary side, the gate drive is suspended. During a fault condition, a smaller turn-off FET slowly brings the gate voltage down.
11	GND_2	Ground Reference for Secondary Side. Connect this pin to the emitter of the IGBT or the source of the MOSFET being driven.
12	V_{OUT_OFF}	Gate Drive Output Current Path for Off Signal.
13	V_{DD2}	Secondary Side Input Supply Voltage, 12 V to 30 V Referenced to GND_2.
14	V_{OUT_ON}	Gate Drive Output Current Path for On Signal.
15	GATE_SENSE	Connect this pin to the gate of power device being driven. This pin senses the gate voltage for the purpose of Miller clamping. When the Miller clamp is not used, tie GATE_SENSE to V_{SS2}.
16	V_{SS2}	Negative Supply for Secondary Side, −15 V to 0 V Referenced to GND_2.

APPLICATIONS INFORMATION

Table 2. Truth Table (Positive Logic)[1]

V_{I+} Input	V_{I-} Input	$\overline{\text{RESET}}$ Pin	READY Pin	$\overline{\text{FAULT}}$ Pin	V_{DD1} State	V_{DD2} State	V_{GATE}
L	L	H	H	H	Powered	Powered	L
L	H	H	H	H	Powered	Powered	L
H	L	H	H	H	Powered	Powered	H
H	H	H	H	H	Powered	Powered	L
X	X	H	L	X	Powered	Powered	L
X	X	H	X	L	Powered	Powered	L
L	L	H	L	X	Unpowered	Powered	L
X	X	L[2]	X	H[2]	Powered	Powered	L
X	X	X	L	X	Powered	Unpowered	Unknown

[1] X = don't care or unknown, L = low, and H = high.
[2] Time dependent value. Refer to **Error! Reference source not found.** section for details on timing.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM4135 IGBT gate driver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DD2}, it is recommended to also add a 10 µF capacitor to provide the charge required to drive the gate capacitance at ADuM4135 outputs. On the output supply pin, avoid the use of vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 5 mm.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay describes the time it takes a logic signal to propagate through a component. The propagation delay to a low output can differ from the propagation delay to a high output. The ADuM4135 specifies t_{DLH} as the time between the rising input high logic threshold (V_{IH}) to the output rising 10% threshold (see Figure 3). Likewise, the falling propagation delay (t_{DHL}) is defined as the time between the input falling logic low threshold (V_{IL}) and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

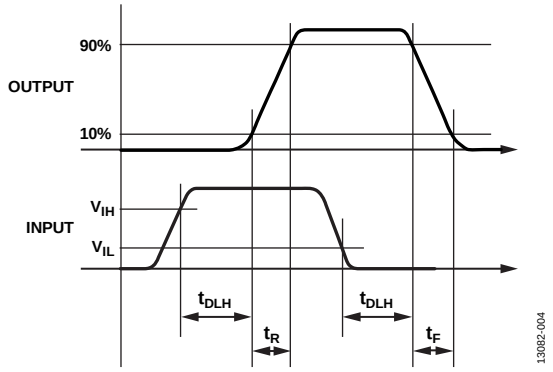

Figure 3. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4135 components operating under the same temperature, input voltage, and load conditions.

PROTECTION FEATURES

Fault Reporting

The ADuM4135 provides protection for faults that may occur during the operation of an IGBT. The primary fault condition is desaturation. If detected, the ADuM4135 shuts down the gate drive and asserts $\overline{\text{FAULT}}$ low. The output remains disabled until $\overline{\text{FAULT}}$ is brought low for more than 500 ns, and then high. $\overline{\text{FAULT}}$ is reset to high on the falling edge of $\overline{\text{FAULT}}$. While $\overline{\text{FAULT}}$ remains held low, the output remains disabled. The $\overline{\text{FAULT}}$ pin has an internal, 300 kΩ pull-down resistor.

Desaturation Detection

Occasionally, component failures or faults occur with the circuitry connected to the IGBT connected to the ADuM4135. Examples include shorts in the inductor/motor windings or shorts to power/ground buses. The resultant excess in current flow causes the IGBT to come out of saturation. To detect this condition and reduce the likelihood of damage to the FET, a threshold circuit

is used on the ADuM4135. If the DESAT pin exceeds the desaturation threshold ($V_{DESAT, TH}$) of 9 V while the high side driver is on, the ADuM4135 enters the failure state and turns the IGBT off. At this time, the $\overline{FAULT}$ pin is brought low. An internal current source of 500 µA is provided, as well as the option to boost the charging current using external current sources or pull-up resistors. The ADuM4135 has a built-in blanking time to prevent false triggering while the IGBT first turns on. The time between desaturation detection and reporting a desaturation fault to the $\overline{FAULT}$ pin is less than 2 µs (t_{REPORT}). Bring $\overline{RESET}$ low to clear the fault. There is a 500 ns debounce ($t_{DEB\_\overline{RESET}}$) on the $\overline{RESET}$ pin. The time shown in Figure 4 as t_{DESAT_DELAY} provides a 300 ns masking time that keeps the internal switch that grounds the blanking capacitor tied low for the initial portion of the IGBT on time.

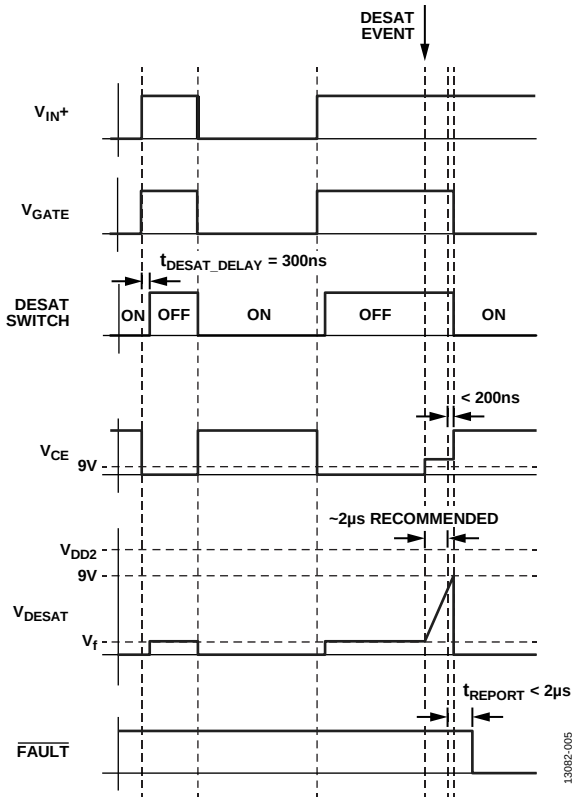

Figure 4. Desaturation Detection Timing Diagram

For the following design example, the schematic in Figure 9 is to be referenced along with the waveforms in Figure 4. Under normal operation, during IGBT off times, the voltage across the IGBT, V_{CE} rises to the rail voltage supplied to the system. In this case, the blocking diode shuts off, protecting the ADuM4135 from high voltages. During the off times, the internal desaturation switch is on, accepting the current going through R_{BLANK}. This allows C_{BLANK} to remain at a low voltage. For the first 300 ns of the IGBT on time, the DESAT switch remains on, clamping the DESAT pin voltage low. After the 300 ns delay time, the DESAT pin is released, and the DESAT pin is allowed to rise to V3? = $V_{CE} + V_F + V_{RDESAT}$. V_{RDESAT} is chosen to dampen the current at this time, usually selected around 100 Ω. Select the blocking diode to block above the high rail voltage on the collector of the IGBT and to be a fast recovery diode.

In the case of a desaturation event, V_{CE} rises above the 9 V threshold in the desaturation detection circuit. The voltage on the DESAT pin rises with an RC time constant profile dependent on C_{BLANK} and R_{BLANK}. The exact timing of this depends on the V3 starting voltage, the V_{DD2} supply voltage, the R_{BLANK} resistor, and the C_{BLANK} capacitor values. Depending on the IGBT specifications, a blanking time of around 2 µs is a typical design choice. When the DESAT pin rises above the 9 V threshold, a fault registers, and within 200 ns, the gate output drives low. The output is brought low using the N-FET fault MOSFET, which is approximately 50 times more resistive than the main gate driver N-FET. This is to perform a soft shutdown to reduce the chance of an over-voltage spike on the IGBT during an abrupt turn-off event. Within 2 µs, the fault is communicated back to the primary side $\overline{FAULT}$ pin. To clear the fault, a reset is required.

Miller Clamp

The ADuM4135 has an integrated Miller clamp to reduce voltage spikes on the IGBT gate due to the Miller capacitance during shut-off of the IGBT. When the input gate signal calls for the IGBT to turn off (driven low), the Miller clamp MOSFET is initially off. When the voltage on the GATE_SENSE pin crosses the 2 V internal voltage reference, as referenced to V_{SS2}, the internal Miller clamp latches on for the remainder of the off time of the IGBT, creating a second low impedance current path for the gate current to follow. The Miller clamp switch remains on until the input drive signal changes from low to high. An example waveform of the timings is shown in Figure 5.

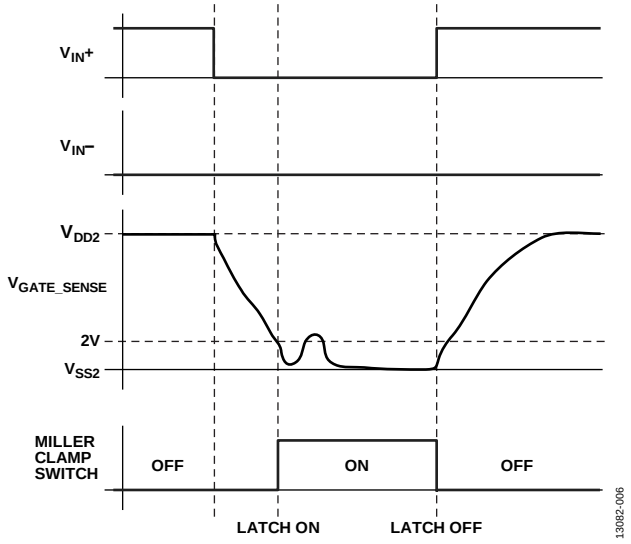

Figure 5. Miller Clamp Example

Thermal Shutdown

If the internal temperature of the ADuM4135 exceeds 145°C (typical), the device enters thermal shutdown (TSD). During this time, the READY pin is brought low on the primary side, and the gate drive is disabled. When TSD occurs, the devices will not leave TSD until the internal temperature drops below 125°C (typical), at which time, the READY pin returns to high, and the device exits shutdown.

Undervoltage lockout (UVLO) Faults

UVLO faults occur when the supply voltages are below the specified UVLO threshold values. During a UVLO event on either the primary side or secondary side, the READY pin goes low, and the gate drive is disabled. When the UVLO condition is removed, the device resumes operation, and the READY pin goes high.

READY Pin

The open-drain READY pin is an output that confirms communication between the primary to secondary sides is active. The READY pin remains high when there are no UVLO or TSD events present. When the READY pin is low, the IGBT gate is driven low.

Table 3.

UVLO	TSD	READY Pin Output
No	No	High
Yes	No	Low
No	Yes	Low
Yes	Yes	Low

$\overline{\text{FAULT}}$ Pin

The open-drain $\overline{\text{FAULT}}$ pin is an output to communicate that a desaturation fault has occurred. While the $\overline{\text{FAULT}}$ pin is low, the IGBT gate is driven low. If a desaturation event occurs, the $\overline{\text{RESET}}$ pin must be driven low for at least 500 ns, then high to return operation to the IGBT gate drive.

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin has an internal 300 kΩ (typical) pull-down resistor. The $\overline{\text{RESET}}$ pin accepts CMOS level logic. When the $\overline{\text{RESET}}$ pin is held low, after a 500 ns debounce time, any faults on the $\overline{\text{FAULT}}$ pin are cleared. While the $\overline{\text{RESET}}$ pin is held low, the switch on V_{OUT_OFF} is closed, bringing the gate voltage of the IGBT low. When $\overline{\text{RESET}}$ is brought high, and no fault exists, the device resumes operation.

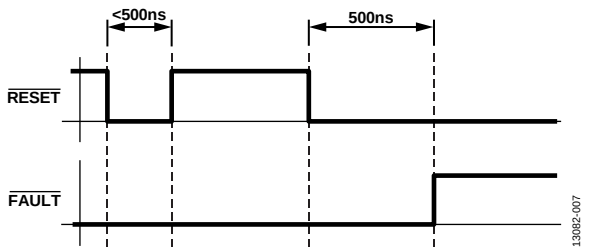

Figure 6. $\overline{\text{RESET}}$ Timing

V_{I+} and V_{I-} Operation

The ADuM4135 has two drive inputs, V_{I+} and V_{I-}, to control the IGBT gate drive signals, V_{OUT_ON} and V_{OUT_OFF}. Both the V_{I+} and V_{I-} use CMOS logic level inputs. The input logic of the V_{I+} and V_{I-} pins can be controlled by either asserting the V_{I+} pin high or the V_{I-} pin low. With the V_{I-} pin low, the V_{I+} pin accepts positive logic. If V_{I+} is held high, the V_{I-} pin accepts negative logic.

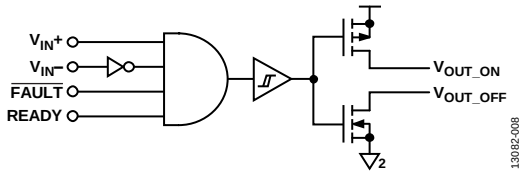

Figure 7. V_{I+} and V_{I-} Block Diagram

Pulses below the deglitch specifications, t_{MIN_IN} and $t_{MIN\_\overline{IN}}$, are ignored. The minimum pulse width, PW, is the minimum period in which the timing specifications are guaranteed. Pulses below the minimum pulse width but above the deglitch time may propagate to the secondary side; however, timing is not guaranteed. See Figure 8 for more details.

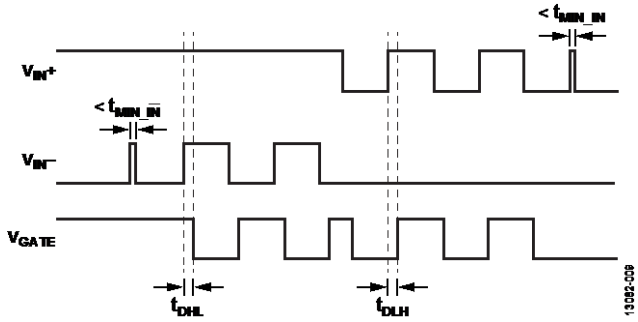

Figure 8. V_{I+} and V_{I-} Timing Diagram.

Gate Resistance Selection

The ADuM4135 provides two output nodes for the driving of an IGBT. The benefit of this approach is that the user can select two different series resistances for the turn-on and turn-off of the IGBT. It is generally desired to have the turn-off occur faster than the turn-on. To select the series resistance, decide what the maximum allowed peak current will be for the IGBT. Knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external resistor can be chosen.

$$I_{PEAK} = (V_{DD2} - V_{SS2})/(R_{DSON\_N} + R_{GOFF})$$

For example, if the turn-off peak current is 4 A, with a (V_{DD2} – V_{SS2}) of 18 V:

$$R_{GOFF} = ((V_{DD2} - V_{SS2}) - I_{PEAK} \times R_{DSON\_N})/I_{PEAK}$$

$$R_{GOFF} = (18\ V - 4\ A \times 0.6\ \Omega)/4\ A = 3.9\ \Omega$$

Once R_{GOFF} is selected, a slightly larger R_{GON} can be selected to arrive at a slower turn-on time.

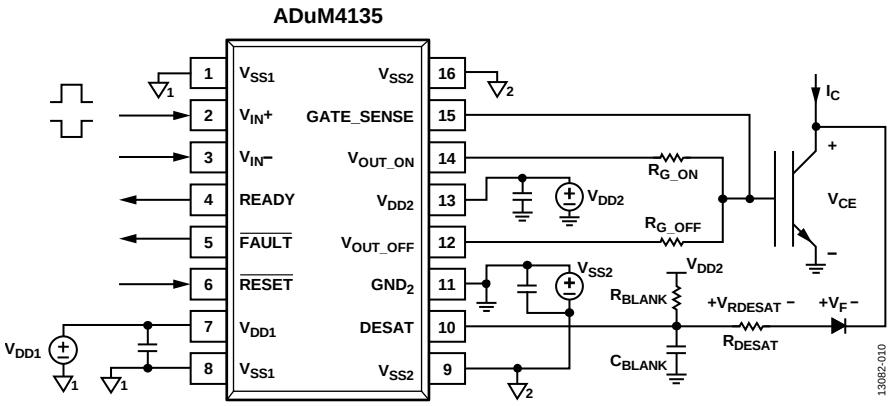

Figure 9. IGBT Drive Example Application

POWER DISSIPATION

During the driving of an IGBT gate, the driver must dissipate power. This power is not insignificant and can lead to thermal shutdown (TSD) if considerations are not made. The gate of an IGBT can be roughly simulated as a capacitive load. Due to Miller capacitance, and other nonlinearities, it is common practice to take the stated input capacitance, C_{ISS}, of a given IGBT, and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation in the system due to switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - V_{SS2})^2 \times f_S$$

where:
$C_{EST} = C_{ISS} \times 5$
f_S is the switching frequency of IGBT.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4135 chip.

$$P_{DISS\_ADuM4135} = P_{DISS} \times 0.5(R_{DSON\_P}/(R_{GON} + R_{DSON\_P})) + (R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

Taking the power dissipation found inside the chip, and multiplying it by the θ_{JA}, gives the rise above ambient temperature that the ADuM4135 experiences.

$$T_{ADuM4135} = \theta_{JA} \times P_{DISS\_ADuM4135} + T_{AMB}$$

For the device to remain within specification, $T_{ADUM4135}$ must not exceed 125°C. If $T_{ADuM4135}$ exceeds 145°C (typical), the device enters thermal shutdown

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4135

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The insulation lifetime of the ADuM4135 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 10, Figure 11, and Figure 12 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross-insulation voltage waveform that does not conform to Note that the voltage presented in Figure 11 is shown as sinusoidal for illustration purposes only. It is meant to represent

any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

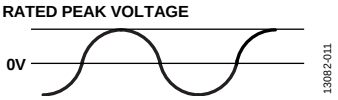

Figure 10. Bipolar AC Waveform

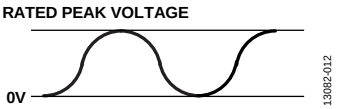

Figure 11. Unipolar AC Waveform

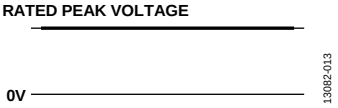

Figure 12. DC Waveform

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4135 is resistant to external magnetic fields. The limitation on the ADuM4135 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 2.3 V operating condition of the ADuM4135 is examined because it represents the most susceptible mode of operation.

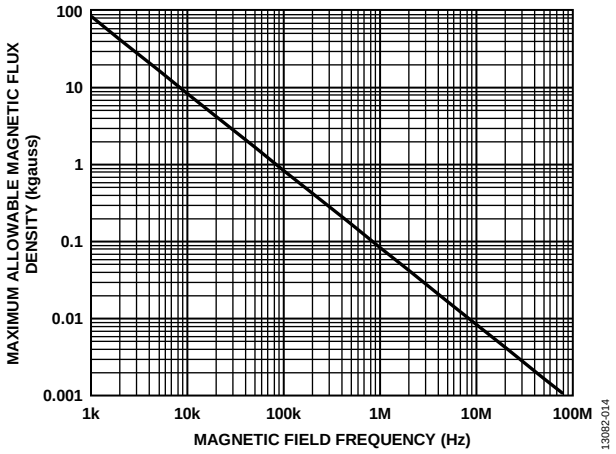

Figure 13. Maximum Allowable External Magnetic Flux Density

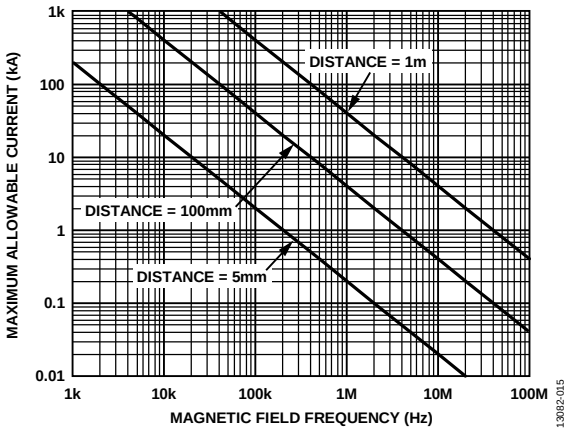

Figure 14. Maximum Allowable Current for Various Current-to-ADuM4135 Spacings

OUTLINE DIMENSIONS

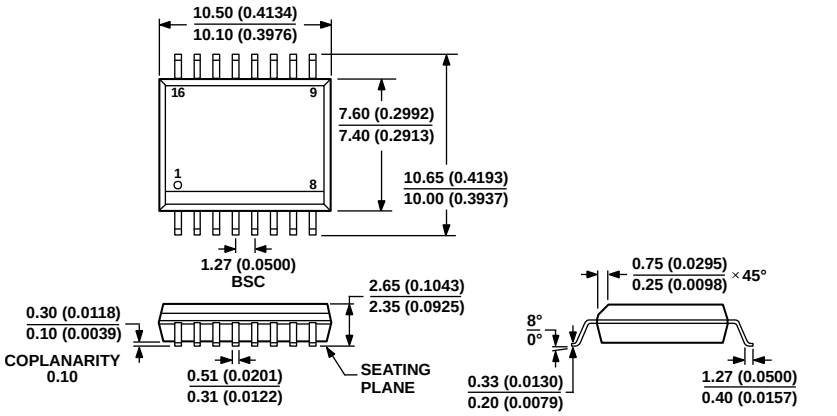

Figure 15. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuM4135RWZ[1]	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
EVAL-ADuM4135EBZ [1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

PR13082-0-5/15(PrA)