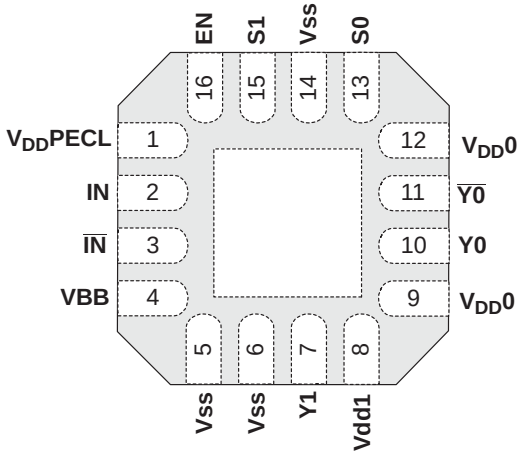
- **Distributes One Differential Clock Input to One LVPECL Differential Clock Output and One LVCMOS Single-Ended Output**
- **Programmable Output Divider for Both LVPECL and LVCMOS Outputs**
- **1.6-ns Output Skew Between LVCMOS and LVPECL Transitions Minimizing Noise**
- **3.3-V Power Supply (2.5-V Functional)**
- **Signaling Rate Up to 800-MHz LVPECL and 200-MHz LVCMOS**
- **Differential Input Stage for Wide Common-Mode Range Also Provides VBB Bias Voltage Output for Single-Ended Input Signals**
- **Receiver Input Threshold ±75 mV**
- **16-Pin QFN Package (3 mm x 3 mm)**

QFN PACKAGE
(TOP VIEW)



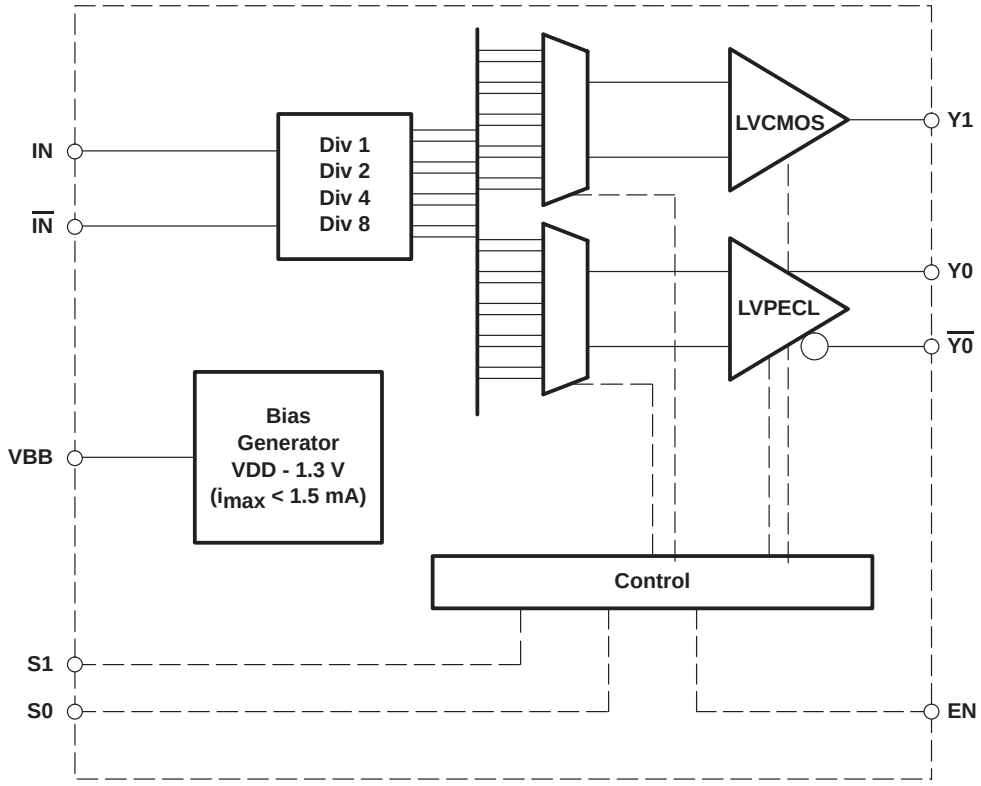
description

The CDCM1802 clock driver distributes one pair of differential clock input to one LVPECL differential clock output pair Y0 and $\overline{Y0}$ and one single-ended LVCMOS output Y1. It is specifically designed for driving 50-Ω transmission lines. The LVCMOS output is delayed by 1.6 ns over the PECL output stage to minimize noise impact during signal transitions.

The CDCM1802 has two control pins, S0 and S1, to select different output mode settings. The S[1:0] pins are 3-level inputs. Additionally, an enable pin EN is provided to disable or enable all outputs simultaneously. The CDCM1802 is characterized for operation from −40°C to 85°C.

For single-ended driver applications, the CDCM1802 provides a VBB output pin that can be directly connected to the unused input as a common-mode voltage reference.

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	16	I (with 60-kΩ pullup)	ENABLE. Enables or disables all outputs simultaneously; The EN pin offers three different configurations: tie to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$) or left floating (logic 1); EN = 1: outputs on according to S0 and S1 setting EN = $V_{DD}/2$: outputs on according to S0 and S1 setting EN = 0; outputs Y[1:0] off (high-impedance) see Table 1 for details.
IN $\overline{IN}$	2 3	I Differential input	Differential input clock. Input stage is sensitive and has a wide common mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Since the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g. with 100-Ω across input). The input can also be driven by a single-ended signal, if the complementary input is tied to a dc reference voltage (e.g. $V_{CC}/2$). The inputs deploy an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~0.7 V. Reverse biasing of the IC through this inputs is possible and must be prevented by limiting the input voltage < VDD
S0 S1	13 15	I I (with 60-kΩ pullup)	Select mode of operation. Defines the output configuration of Y0 and Y1. Each pin offers three different configurations: tied to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$) or left floating (logic 1); see Table 1 for details
Y1	7	O	LVCMOS clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S0, S1, and EN. Also, this output can be disabled by tying $V_{DD}1$ to GND.
Y0 $\overline{Y0}$	10 11	O LVPECL	LVPECL clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S1, S0, and EN. If Y0 output is unused, the output can simply be left open to save power and minimize noise impact to Y1.
VBB	4	O	Output bias voltage used to bias unused complementary input $\overline{IN}$ for single-ended input signals. The output voltage of VBB is V_{DD} −1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{SS}	5, 6, 14	Supply	Device ground
V_{DD}PECL	1	Supply	Supply voltage PECL input + internal logic
$V_{DD}0$	9, 12	Supply	PECL output supply voltage for output Y0; Y0 can be disabled by pulling $V_{DD}0$ to GND. Caution: In this mode no voltage from outside may be forced because internal diodes could be forced in a forward direction. Thus, it is recommended to leave the output disconnect
$V_{DD}1$	8	Supply	Supply voltage CMOS output; The CMOS output can be disabled by pulling $V_{DD}1$ to GND. Caution: In this mode no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to leave Y1 unconnected, tied to GND or terminated into GND

control pin settings

The CDCM1802 has three control pins, S0, S1, and the enable pin (EN) to select different output mode settings. All three inputs (S0, S1, EN) are 3-level inputs. In addition, the EN input allows disabling all outputs and place them into a high-z (or tristate) output state when pulled to GND.

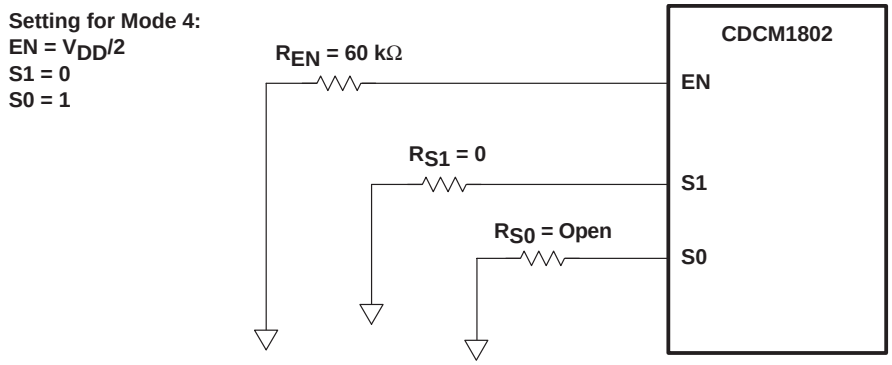


Figure 1. Control Pin Setting for Example

Each control input incorporates a 60-kΩ pullup resistor. Thus, it is easy to choose the input setting by designing a resistor pad between the control input and GND. To choose a logic zero, the resistor value must be zero. Setting the input high requires leaving the resistor pad empty (no resistor installed). For setting the input to $V_{DD}/2$, the installed resistor needs a value of 60 kΩ with a tolerance better or equal to 10%.

Table 1. Selection Mode Table

				LVPECL	LVCMOS
MODE	EN	S1	S0	Y0	Y1
0	0	X	X	Off (high-z)	Off (high-z)
1	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 1
2	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 2
3	1	0	0	÷ 1	÷ 4
4	$V_{DD}/2$	0	1	÷ 2	÷ 2
5	1	0	1	÷ 2	÷ 4
6	$V_{DD}/2$	0	0	÷ 4	÷ 4
7	$V_{DD}/2$	1	0	÷ 4	÷ 8
8	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 8	÷ 1
9	1	1	0	÷ 8	÷ 4
10	1	1	1	Off (high-z)	÷ 4

NOTE: The LVPECL outputs are open emitter stages. Thus, if you leave the unused LVPECL output Y0 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

V_{DD}	Supply voltage	−0.3 V to 3.8 V
V_I	Input voltage	−0.2 V to (V_{DD} +0.2 V)
V_O	Output voltage	−0.2 V to (V_{DD} +0.2 V)
Yn, $\overline{Yn}$, I_{OSD}	Differential short circuit current	Continuous
ESD	Electrostatic discharge (HBM 1.5 kΩ, 100 pF)	>2000 V
	Moisture level 16-pin QFN package (solder reflow temperature of 235°C) MSL	1
T_{stg}	Storage temperature	−65°C to 150°C
T_J	Maximum junction temperature	125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Supply voltage, V_{DD} (only functionality)	2.375		3.6	V
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT IN, $\overline{IN}$						
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD}−0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$, See Note 1		500		1300	mV
V_{IN}	Input voltage swing between IN and $\overline{IN}$, See Note 2		150		1300	mV
I_{IN}	Input current	V_I = V_{DD} or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF
LVPECL OUTPUT DRIVER Y0, $\overline{Y0}$						
f_{clk}	Output frequency, See Figure 4		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD}−2 V	V_{DD}−1.18		V_{DD}–0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD}−2 V	V_{DD}−1.98		V_{DD}–1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$, See Figure 4	Termination with 50 Ω to V_{DD}−2 V	500			mV
I_{OZL}	Output 3-state	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}	Output 3-state	V_{DD} = 3.6 V, V_O = V_{DD} – 0.8 V			10	µA
t_r/t_f	Rise and fall time	20% to 80% of V_{OUTPP}, see Figure 9	200		350	ps
t_{Duty}	Output duty cycle distortion, See Note 3	Crossing point-to-crossing point distortion	−50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y0, See Note A in Figure 8		50		ps
C_O	Output capacitance	V_O = V_{DD} or GND		1		pF
LOAD	Expected output load			50		Ω

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT-TO-LVPECL OUTPUT PARAMETER						
$t_{pd(lh)}$	Propagation delay rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew, See Note B in Figure 8	VOX to VOX			100	ps

NOTES: 1. Is required to maintain ac specifications
2. Is required to maintain device functionality
3. For a 800-MHz signal, the 50-ps error would result into a duty cycle distortion of ±4% when driven by an ideal clock input signal.

LVCMOS OUTPUT PARAMETER, Y1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Note 4 and Figure 5			0		200	MHz
$t_{skLVCMOS(o)}$	Output skew between the LVCMOS output Y1 and LVPECL output Y0	VOX to V_{DD}/2, See Figure 8			1.6		ns
$t_{sk(pp)}$	Part-to-part skew	Y1, See Note A in Figure 8			300		ps
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = −100 μA	V_{DD}–0.1			V
		V_{DD} = 3 V,	I_{OH} = −6 mA	2.4			
		V_{DD} = 3 V,	I_{OH} = −12 mA	2			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL}=100 μA			0.1	V
		V_{DD} = 3 V,	I_{OL} = 6 mA			0.5	
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		−29		mA
I_{OL}	Low-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		37		mA
I_{OZ}	High-impedance state output current	V_{DD} = 3.6 V,	V_O = V_{DD} or 0 V			±5	μA
C_O	Output capacitance	V_{DD} = 3.3 V			2		pF
Load	Expected output loading, see Figure 10				10		pF
t_{Duty}	Output duty cycle distortion, see Note 5	Measured at V_{DD}/2		−150		150	ps
$t_{pd(lh)}$	Propagation delay rising edge from IN to Y1	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
$t_{pd(hl)}$	Propagation delay falling edge from IN to Y1	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
t_r	Output rise slew rate	20% to 80% of swing, see Figure 10		1.4	2.3		V/ns
t_f	Output fall slew rate	80% to 20% of swing, see Figure 10		1.4	2.3		V/ns

NOTES: 4. Operating the CDCM1802 LVCMOS output above the maximum frequency will not cause a malfunction to the device, but the Y1 output signal swing will not achieve enough signal swing to meet the output specification. Therefore, the CDCM1802 can be operated at higher frequencies, while the LVCMOS output Y1 becomes unusable.
5. For a 200-MHz signal, the 150-ps error would result in a duty cycle distortion of ±3% when driven by an ideal clock input signal.

jitter characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y0, See Figure 2	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.15	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.25	
$t_{jitterLVCMOS}$	Additive phase jitter from input to LVCMOS output Y1, See Figure 3	12 kHz to 20 MHz, f_{out} = 250 MHz, divide by 1 mode			0.25	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz, divide by 1 mode			0.4	ps rms

ADDITIVE PHASE NOISE vs FREQUENCY OFFSET FROM CARRIER − LVPECL

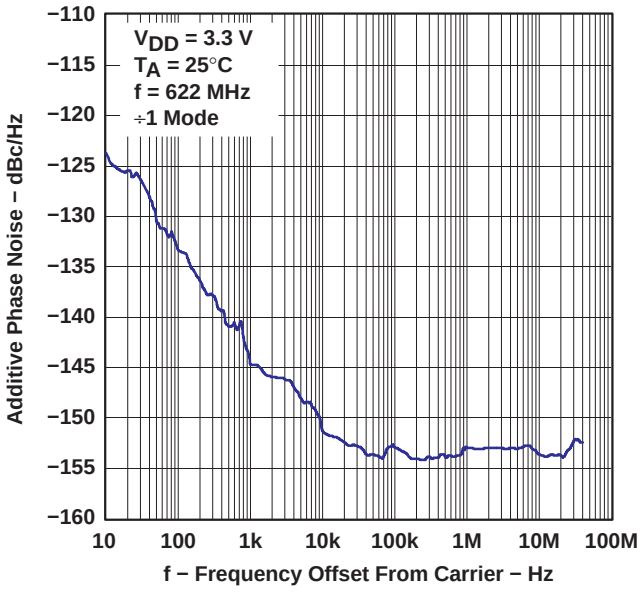


Figure 2

ADDITIVE PHASE NOISE vs FREQUENCY OFFSET FROM CARRIER − LVCMOS

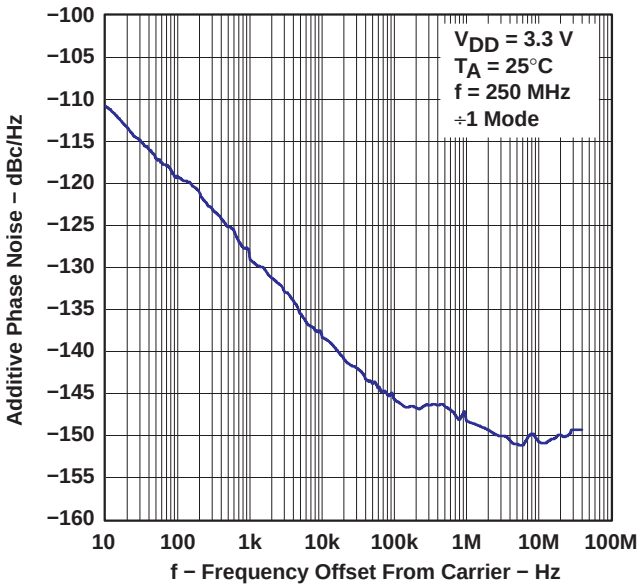


Figure 3

jitter characteristics (continued)

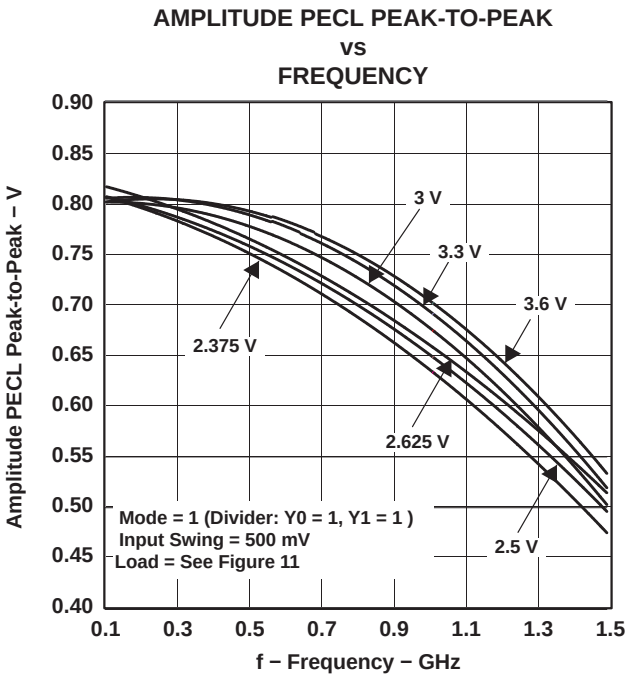


Figure 4

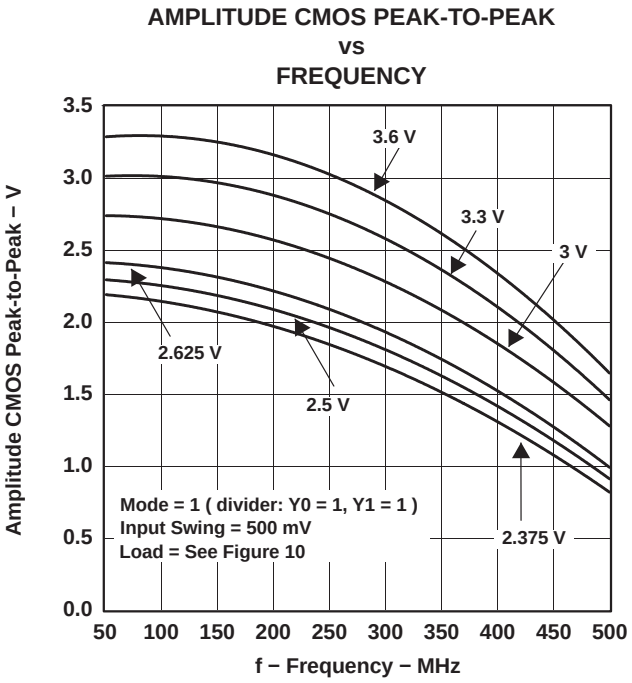
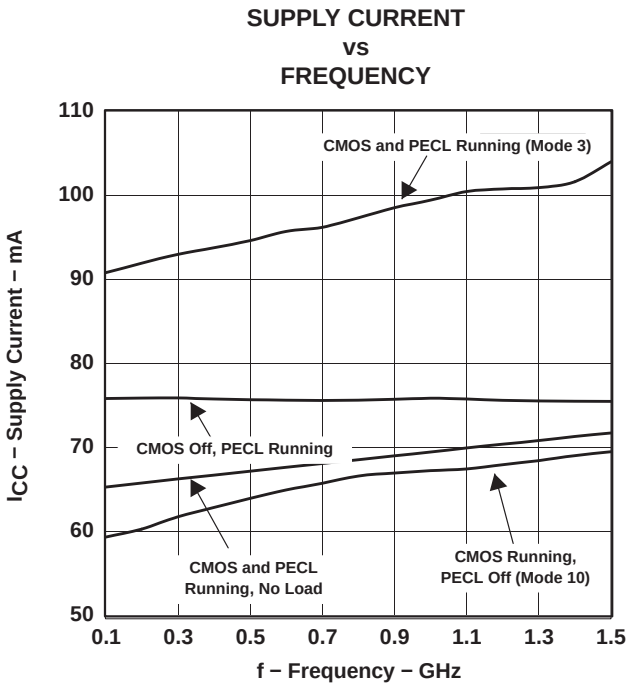


Figure 5

supply current electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} − 2 V on LVPECL outputs and 10 pF on LVCMOS output, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.3 V		100		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.6 V			85	
I_{DDZ}	Supply current, 3-state		All outputs 3-state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA



NOTE: Input swing = 500 mV

Figure 6

Package Thermal Resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	QFN−16 package thermal resistance with thermal vias in PCB, See Note 1	4-layer JEDEC test board (JESD51−7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		40.8		°C/W

NOTE 1: It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 85°C (temperature of the chassis)

$P_{effective} = I_{max} \times V_{max}$ = 85 mA x 3.6 V = 306 mW (max power consumption inside the package)

$\Delta T_{Junction} = \theta_{JA} \times P_{effective}$ = 40.8°C/W x 306 mW = 12.48°C

$T_{Junction} = \Delta T_{Junction} + T_{Chassis}$ = 12.48°C + 85°C = 97.48°C (the maximum junction temperature of $T_{die-max}$ = 125°C is not violated)

control input characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{su}	Setup time, S0, S1, and EN pin before clock IN		25			ns
t_h	Hold time, S0, S1, and EN pin after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		µs
Rpullup	Internal pullup resistor on S0, S1, and EN input		42	60	78	kΩ
$V_{IH(H)}$	Three level input high, S0, S1, and EN pin, see Note 1		$0.9xV_{DD}$			V
$V_{IM(M)}$	Three level input MID, S0, S1, and EN pin		$0.3xV_{DD}$		$0.7xV_{DD}$	V
$V_{IL(L)}$	Three level low, S0, S1, and EN pin				$0.1xV_{DD}$	V
I_{IH}	Input current, S0, S1, and EN pin	$V_I = V_{DD}$			−5	µA
I_{IL}	Input current, S0, S1, and EN pin	V_I = GND	38		85	µA

NOTES: 1. Leaving this pin floating automatically pulse the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

bias voltage VBB over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VBB	Output reference voltage	V_{DD} = 3 V − 3.6 V, I_{BB} = −0.2 mA	V_{DD} − 1.4		V_{DD} − 1.2	V

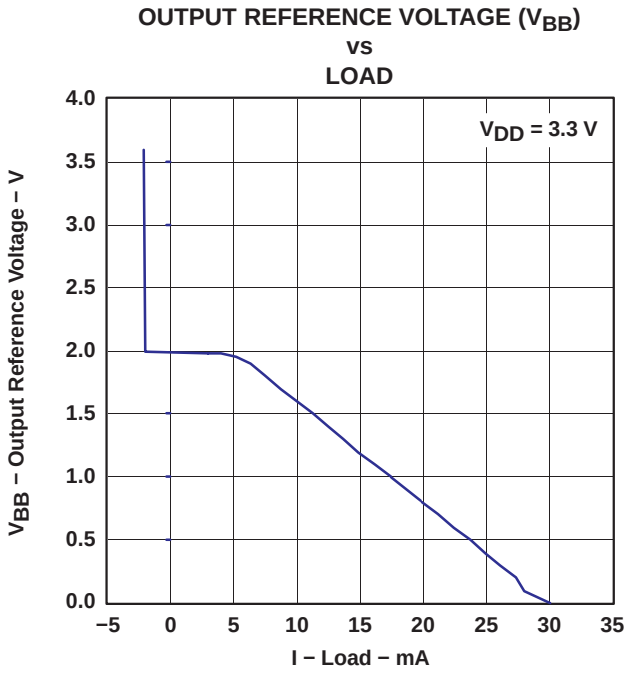
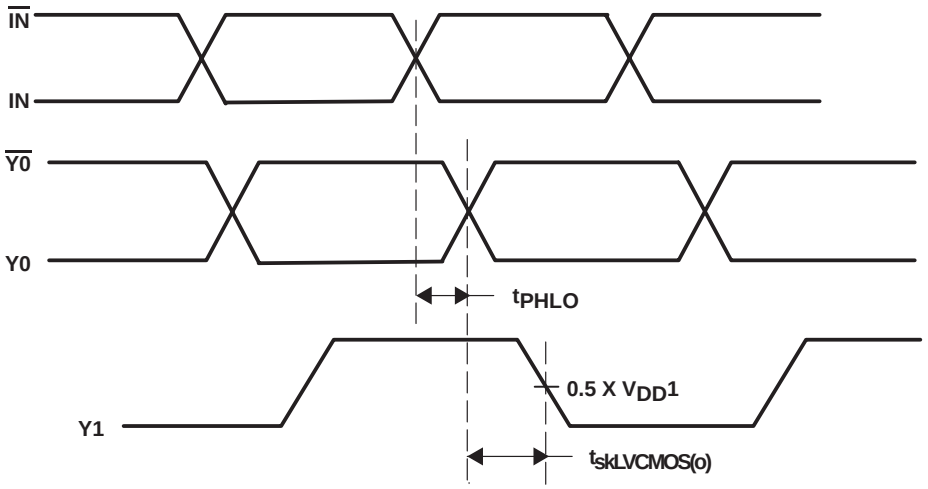


Figure 7

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ across multiple devices
- The difference between the fastest and the slowest $t_{pd(HL)n}$ across multiple devices

B. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes Y0 to switch, $t_{sk(p)} = |t_{pd(HL)} - t_{pd(LH)}|$. Pulse skew is sometimes referred to as *pulse width distortion* or *duty cycle skew.*

Figure 8. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

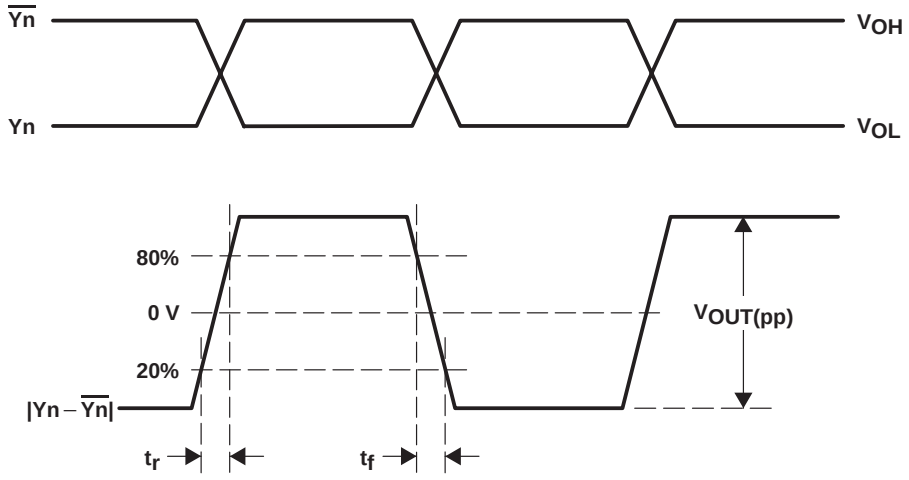


Figure 9. LVPECL Differential Output Voltage and Rise/Fall Time

PARAMETER MEASUREMENT INFORMATION

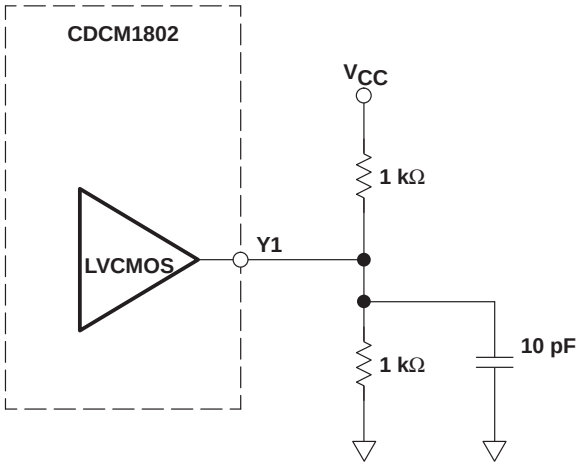


Figure 10. LVCMOS Output Loading During Device Test

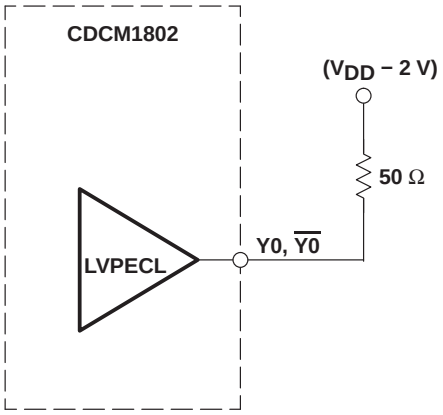


Figure 11. LVPECL Output Loading During Device Test

PCB design for thermal functionality

It is recommended to take special care of the PCB design for good thermal flow from the QFN−16 pin package to the PCB. The current consumption of the CDCM1802 is fixed. JEDEC JESD51−7 specifies thermal conductivity for standard PCB boards.

Modeling the CDCM1802 with a 4−layer JEDEC board (including four thermal vias) results into 37.5°C max temperature with a θ_{JA} of 40.84°C for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications.

PARAMETER MEASUREMENT INFORMATION

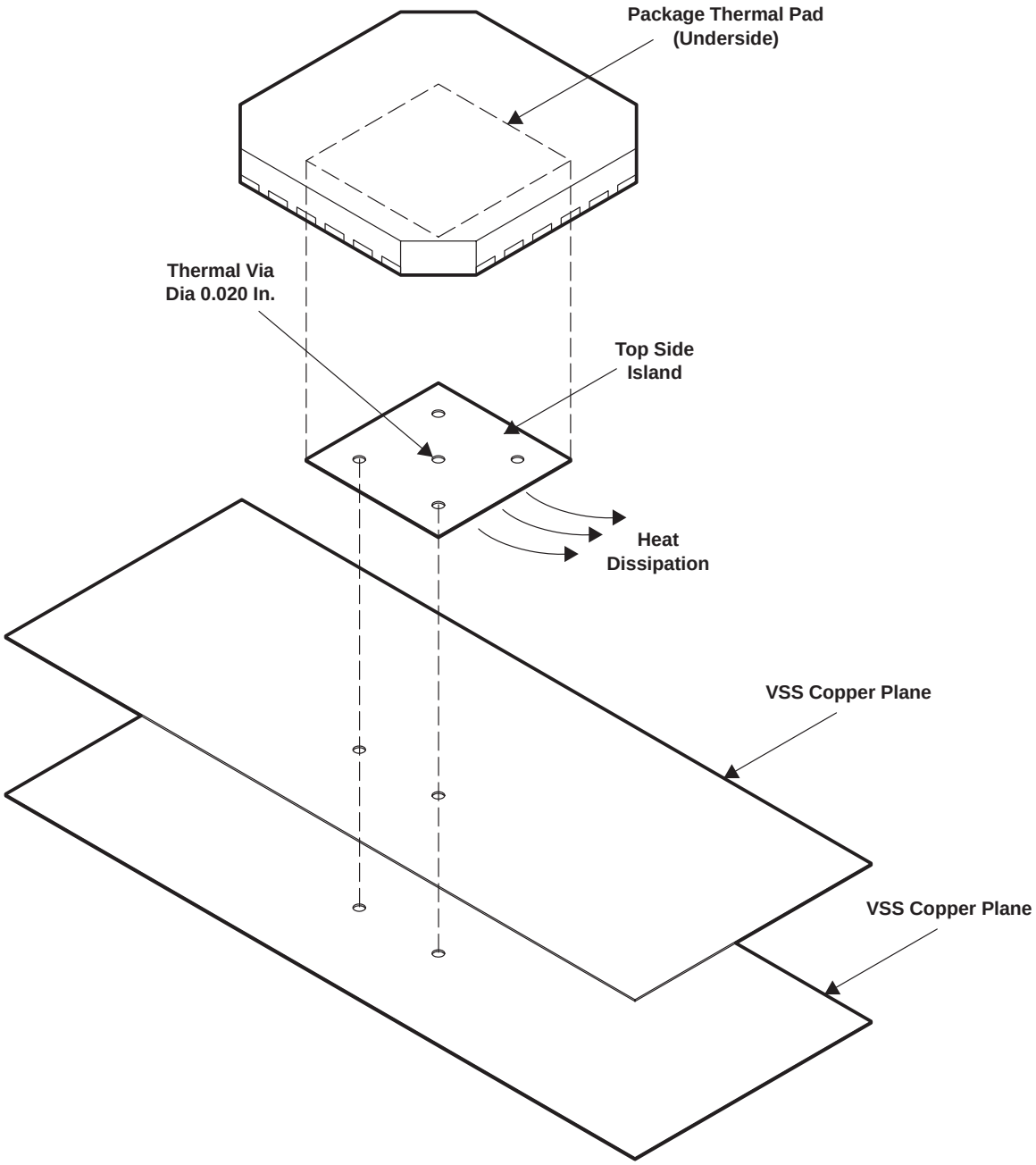


Figure 12. Recommended Thermal Via Placement

See the SCBA017 and the SLUA271 application notes for further package related information.

APPLICATION INFORMATION

LVPECL receiver input termination

The input of the CDCM1802 has high impedance and comes with a very large common mode voltage range. For optimized noise performance it is recommended to properly terminate the PCB trace (transmission line).

Additional termination techniques can be found in the following application notes: SCAA062 and SCAA059.

http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.jhtml?abstractName=scaa062

http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.jhtml?abstractName=scaa059

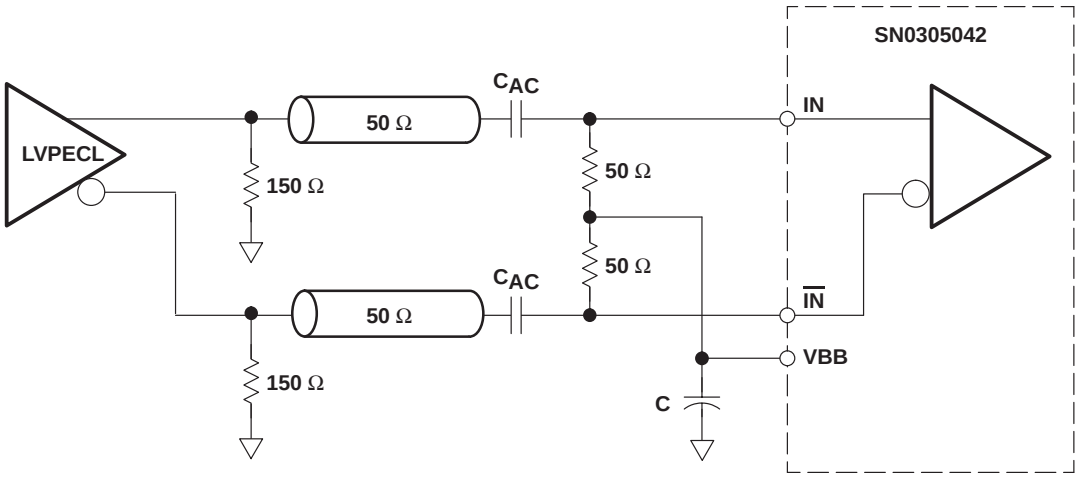


Figure 13. Recommended AC-Coupling LVPECL Receiver Input Termination

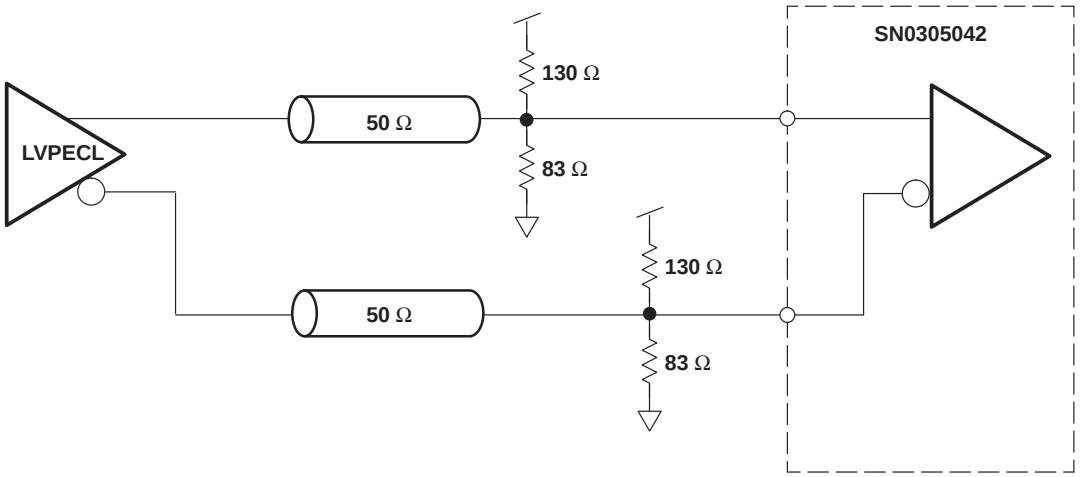
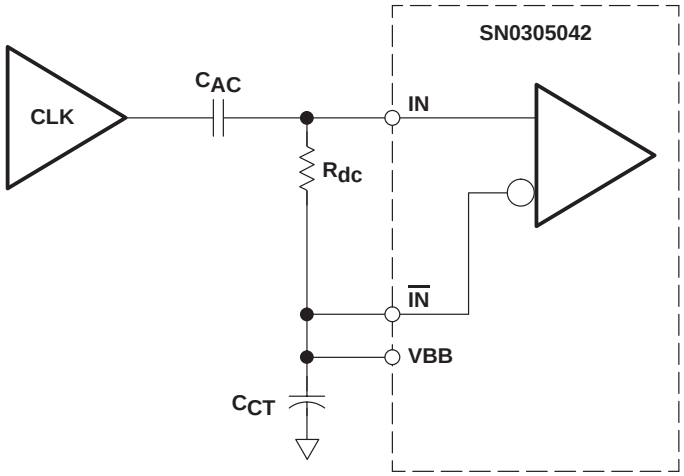


Figure 14. Recommended DC-Coupling LVPECL Receiver Input Termination

APPLICATION INFORMATION



NOTE: C_{AC} − AC-coupling capacitor (e.g., 10 nF)
C_{CT} − Capacitor keeps voltage at $\overline{IN}$ constant (e.g., 10 nF)
R_{dc} − Load and correct duty cycle (e.g., 50 Ω)
V_{BB} − Bias voltage output

Figure 15. Typical Application Setting for Single-Ended Input Signals Driving the SN0305042

device behavior during RESET and control pin switching

output behavior when enabling the device (EN = 0 ⇒ 1)

In disable mode (EN = 0), all output drivers are switched in high-Z mode. The bandgap, current references, the amplifier, and the S0 and S1 control inputs are also switched off. In the same mode, all flip-flops will be reset. The typical current consumption is likely below 500 µA (to be measured).

When the device will be enabled again it takes maximal 1 µs for the settling of the reference voltage and currents. During this time the output Y0 and $\overline{Y0}$ drive a high signal. Y1 is unknown (could be high or low). After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device look like those shown in Figure 16. The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.

APPLICATION INFORMATION

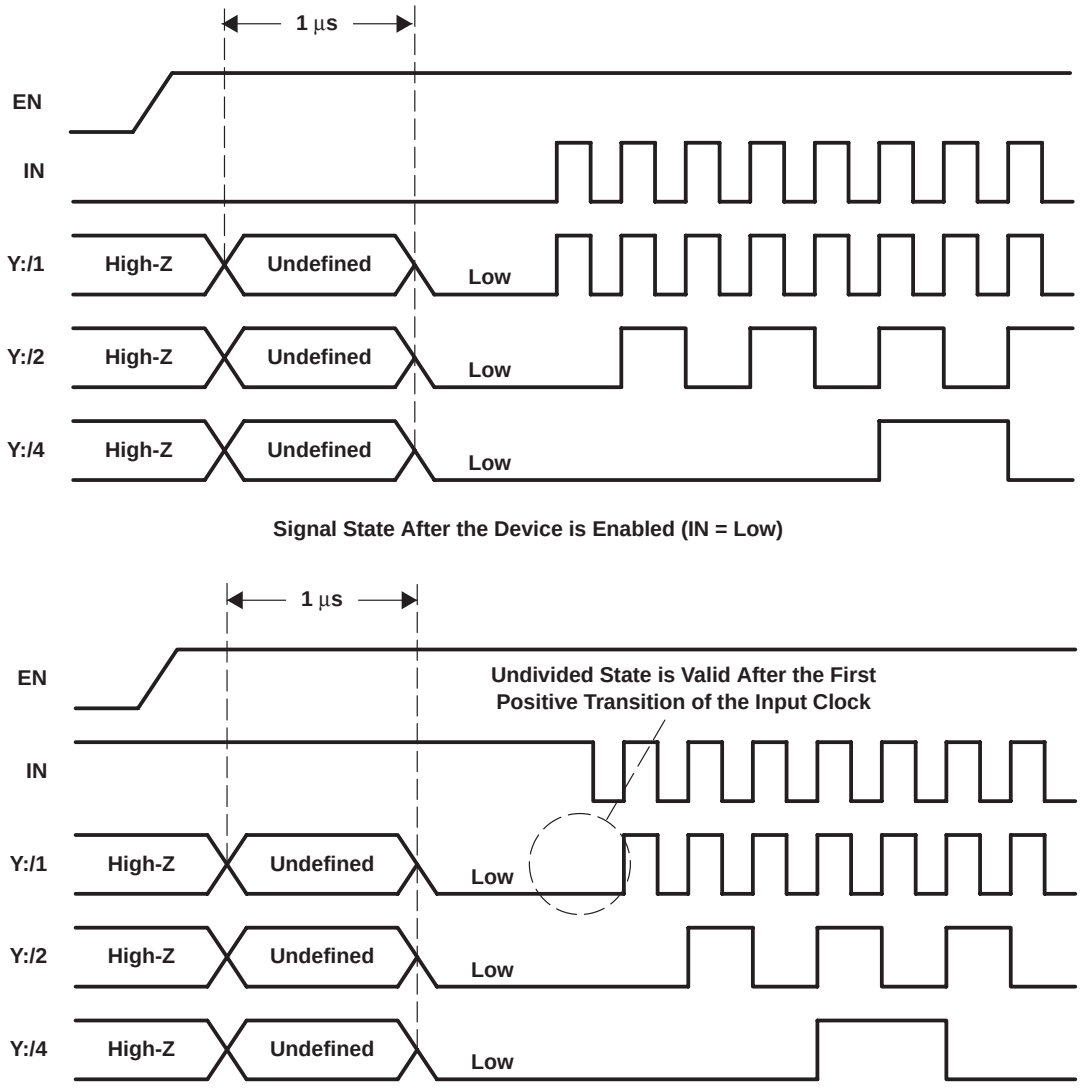


Figure 16. Waveforms

APPLICATION INFORMATION

enabling a single output stage

If a single output stage becomes enabled:

1. Y0 will either be low or high (undefined).
2. $\overline{Y0}$ will be the inverted signal of Y0.

With the first positive clock transition, the undivided output becomes the input clock state. If a divide mode is used, the divided output states are equal to the actual internal divider. The internal divider does not get a reset while enabling single output drivers.

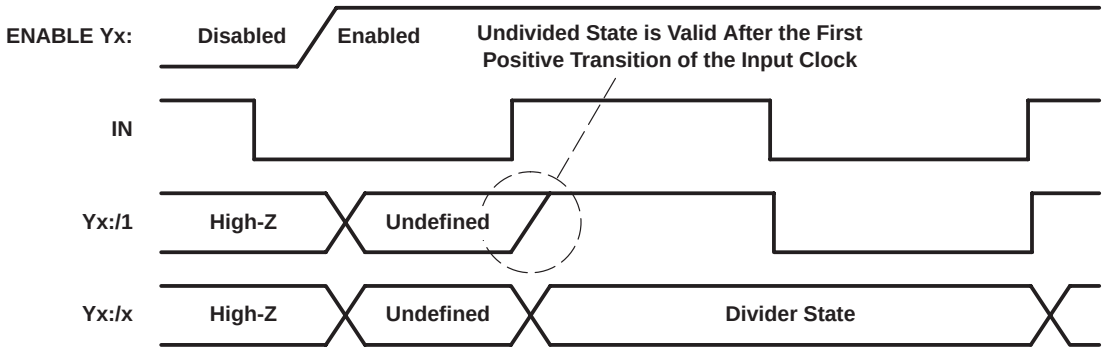


Figure 17. Signal State After an Output Driver Becomes Enabled While IN = 0

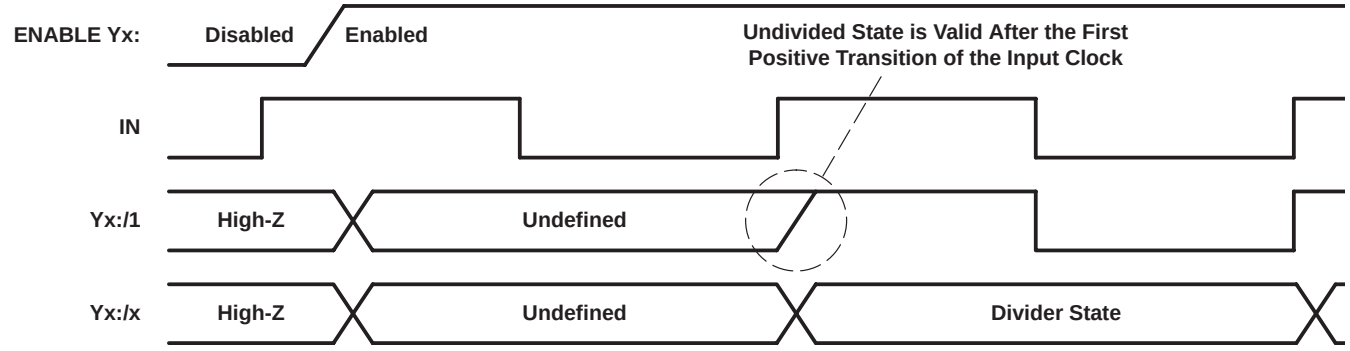


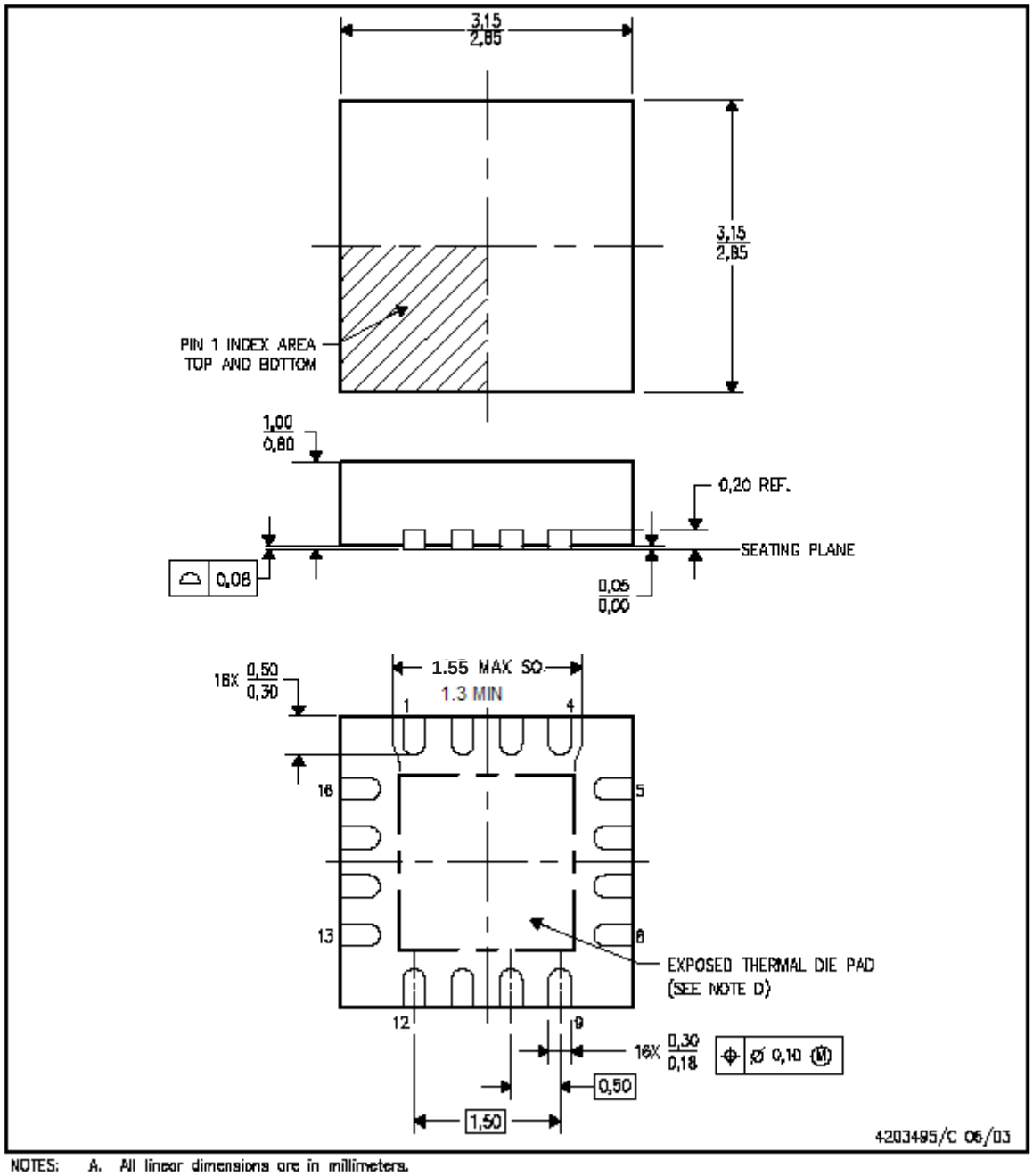
Figure 18. Signal State After an Output Driver Becomes Enabled While IN = 1

MECHANICAL DATA

Also see the following two application notes for further package related information.

http://focus.ti.com/lit/an/scba017c/scba017c.pdf
http://focus.ti.com/lit/an/slua271/slua271.pdf

RGT (S–PQFP–N16) **PLASTIC QUAD FLATPACK**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC MO–220.

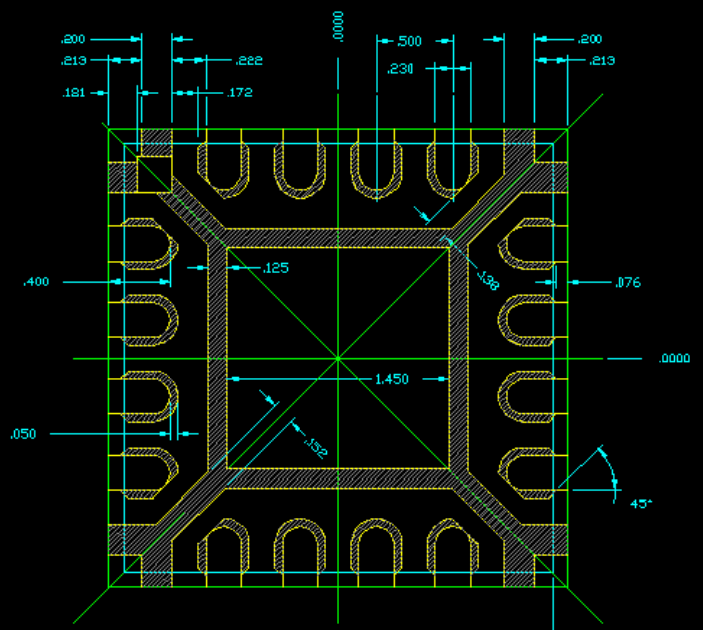
NOTES : UNLESS OTHERWISE SPECIFIED

		STAMPING	ETCHING
1 .	UNSPECIFIED CRITERIA INSPECT PER FAIM 02500 AT	-NA-	YES
2 .	ALL SPECIFIED CRITERIA APPLICABLE TO FINISHED PRODUCT		
3 .	MATERIAL THICKNESS	.200	±.008
4 .	RADIUS ON ALL CORNER UNLESS OTHERWISE SPECIFIED	.152 MAX	
5 .	DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINE EXCEPT AS SHOWN		
6 .	ALL DIMENSIONS IN MM		

PLATING THICKNESS : 125 MICRO INCH MIN SPOT Ag

OPTION TABLE :

OPT. #	PAD SIZE	BLOCK SIZE	MATERIAL TYPE	
01A	1.45mm X 1.45mm	52mm X 52mm	C194 FH	



16L (3X3 BODY)
1.45mm X 1.45mm EXPOSED PAD
0.5mm PITCH
SCALE : 30X

NOTES:
CROSS HATCH AREA HALF-ETCH FROM BOTTOM

CARSEM SEMICONDUCTOR SDN. BHD.
A Member of the Hong Leong group Malaysia

TOLERANCES UNITS = MM	
2 PLS	N/A
3 PLS	±.051
4 PLS	±.0254
ANG°	±1°

DRAWN: DATE:
CHKED: DATE:
FORMERLY: -NA-

TITLE
MLP QUAD (52mm SQ BLOCK)
16L 3X3 BODY
1.45mm X 1.45 EXPOSE PAD

DRAWING LAYOUT NAME	COMPUTER FILENAME
cover	TR42381B.DWG

SHEET	SIZE	DWG #	REV.
1 OF 1	A	TR42381	B

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