- **TTL-Compatible Input Levels**

**D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)**

1$\overline{\text{OE}}$	1	16	V$_{CC}$
S1	2	15	2$\overline{\text{OE}}$
1B4	3	14	S0
1B3	4	13	2B4
1B2	5	12	2B3
1B1	6	11	2B2
1A	7	10	2B1
GND	8	9	2A

**RGY PACKAGE
(TOP VIEW)**

Pins: 1$\overline{\text{OE}}$ (1), V$_{CC}$ (16), S1 (2), 1B4 (3), 1B3 (4), 1B2 (5), 1B1 (6), 1A (7), GND (8), 2A (9), 2B1 (10), 2B2 (11), 2B3 (12), 2B4 (13), S0 (14), 2$\overline{\text{OE}}$ (15)
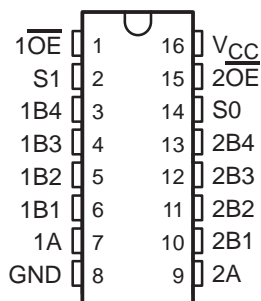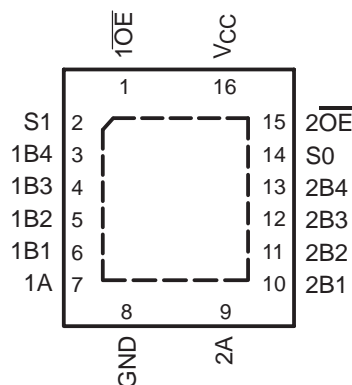
description/ordering information

The SN74CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$, S0, and S1 select the appropriate B output for the A-input data.

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3253RGYR	CU253
	SOIC – D	Tube	SN74CBT3253D	CBT3253
		Tape and reel	SN74CBT3253DR	
	SSOP – DB	Tape and reel	SN74CBT3253DBR	CU253
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3253DBQR	CU253
	TSSOP – PW	Tube	SN74CBT3253PW	CU253
		Tape and reel	SN74CBT3253PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				FUNCTION
1$\overline{\text{OE}}$	2$\overline{\text{OE}}$	S1	S0	
X	H	X	X	Disconnect 1A and 2A
H	X	X	X	Disconnect 1A and 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)
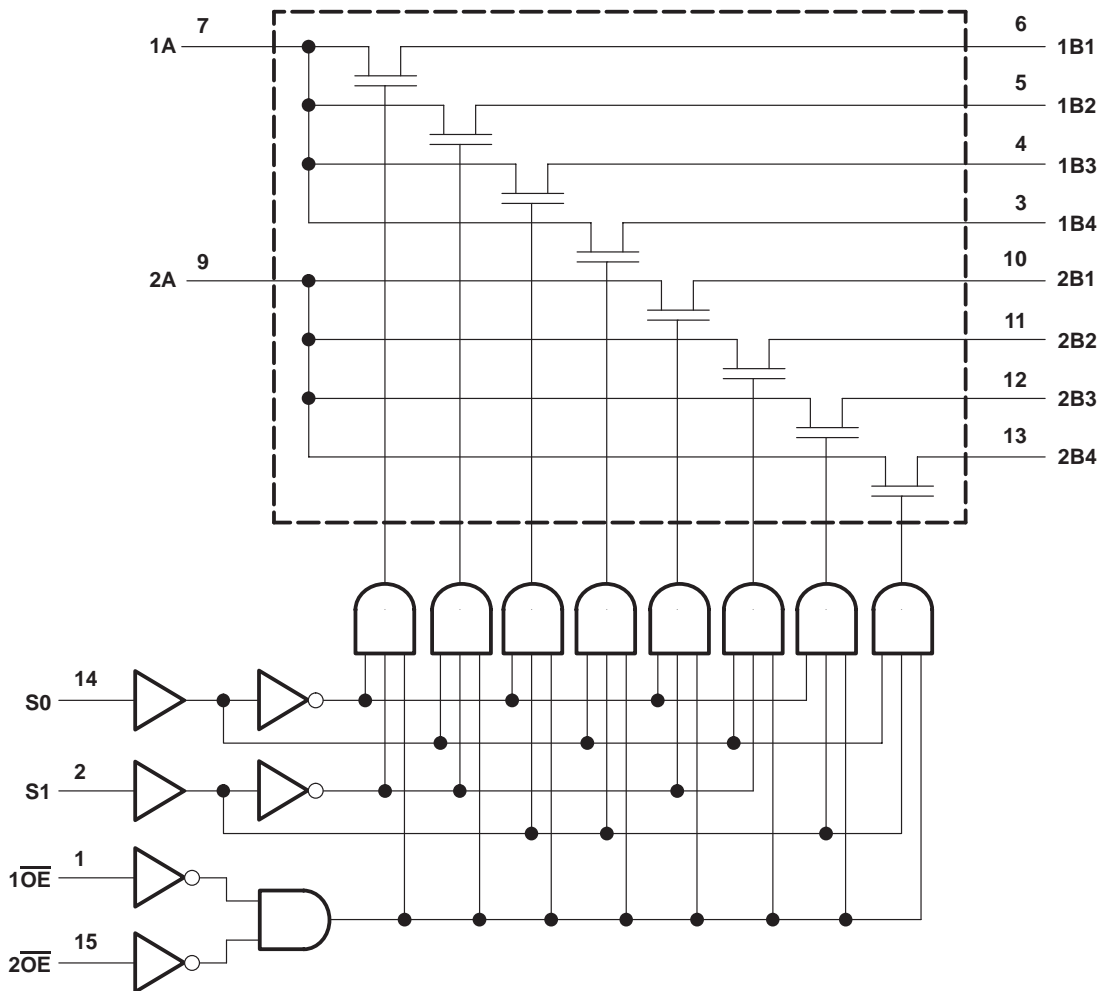
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Continuous channel current .... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 73°C/W
　　　　　　　　　　　(see Note 2): DB package .... 82°C/W
　　　　　　　　　　　(see Note 2): DBQ package .... 90°C/W
　　　　　　　　　　　(see Note 2): PW package .... 108°C/W
　　　　　　　　　　　(see Note 3): RGY package .... 39°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
　　　　2. The package thermal impedance is calculated in accordance with JESD 51-7.
　　　　3. The package thermal impedance is calculated in accordance with JESD 51-5.

TEXAS INSTRUMENTS

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			10		pF
	B port					4		
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

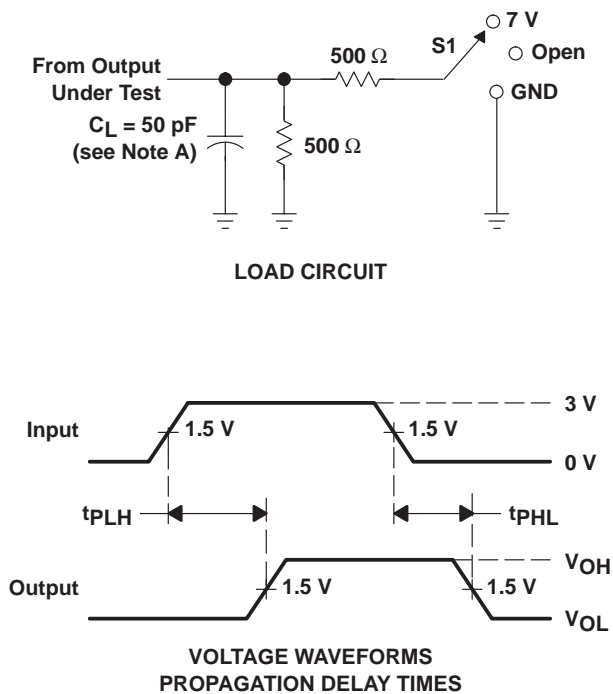| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{pd}	S	A or B		6.6	1.6	6.2	ns
t_{en}	S	A or B		7.1	1.3	6.3	ns
	$\overline{OE}$			7.3	1.4	6.4	
t_{dis}	S	A or B		7.9	1.1	7.4	ns
	$\overline{OE}$			7.3	2.3	7	

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
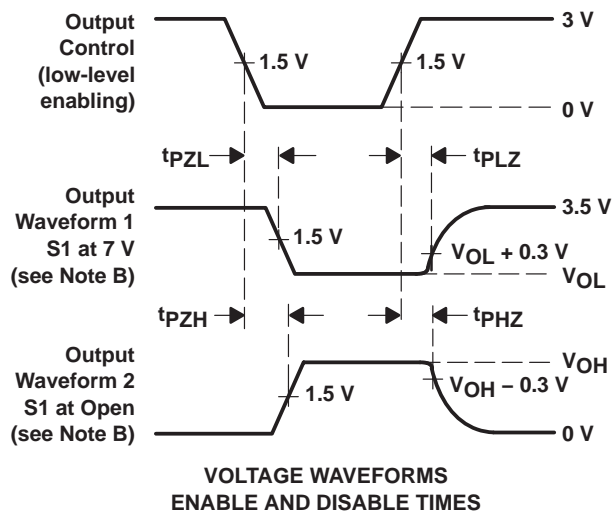
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

From Output Under Test — 500 Ω — S1 — 7 V / Open / GND

C_L = 50 pF (see Note A)

500 Ω

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

Input: 1.5 V ... 1.5 V ... 3 V / 0 V

t_{PLH} ... t_{PHL}

Output: 1.5 V ... 1.5 V ... V_{OH} / V_{OL}

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

Output Control (low-level enabling): 1.5 V ... 1.5 V ... 3 V / 0 V

t_{PZL} ... t_{PLZ}

Output Waveform 1 S1 at 7 V (see Note B): 1.5 V ... 3.5 V / V_{OL} + 0.3 V / V_{OL}

t_{PZH} ... t_{PHZ}

Output Waveform 2 S1 at Open (see Note B): 1.5 V ... V_{OH} / V_{OH} − 0.3 V / 0 V

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PHL} and t_{PLH} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74CBT3253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253DBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
SN74CBT3253DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3253DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3253DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3253DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74CBT3253PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3253RGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3253RGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
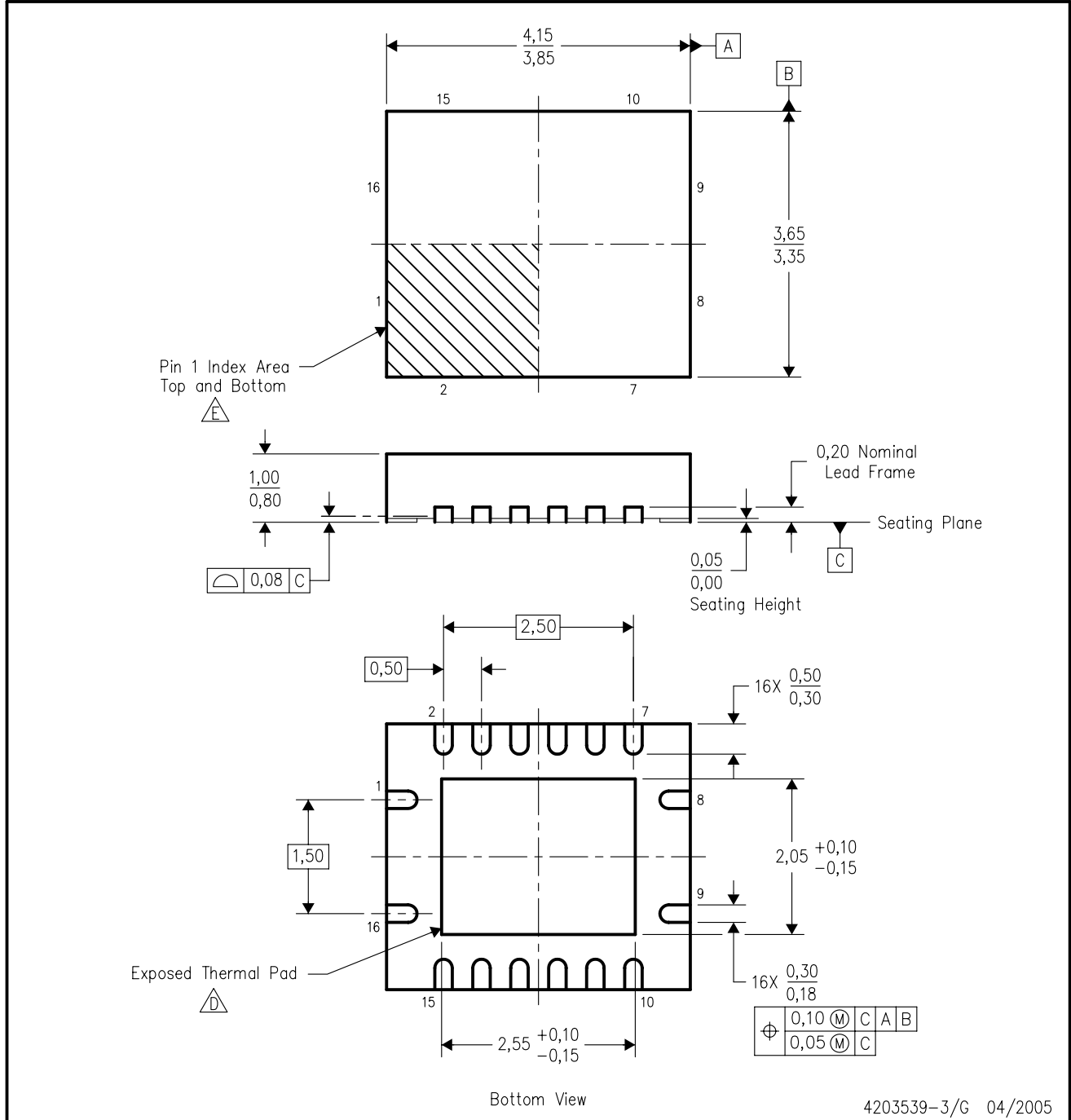
D (R−PDSO−G16)   **PLASTIC SMALL−OUTLINE PACKAGE**

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed .006 (0,15) per end.
         ⚠D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E. Reference JEDEC MS−012 variation AC.

TEXAS INSTRUMENTS
www.ti.com

RGY (R-PQFP-N16)   **PLASTIC QUAD FLATPACK**

$\frac{4,15}{3,85}$ A

B

15   10

16

9

$\frac{3,65}{3,35}$

Pin 1 Index Area
Top and Bottom

⟨E⟩

1

2   7

$\frac{1,00}{0,80}$

0,20 Nominal
Lead Frame

Seating Plane

⎵ 0,08 C

$\frac{0,05}{0,00}$
Seating Height

C

2,50

0,50

16X $\frac{0,50}{0,30}$

2   7

1

8

1,50

2,05 $^{+0,10}_{-0,15}$

16

9

Exposed Thermal Pad

⟨D⟩

15   10

2,55 $^{+0,10}_{-0,15}$

16X $\frac{0,30}{0,18}$

⌖ | 0,10 Ⓜ | C | A | B
⌖ | 0,05 Ⓜ | C

Bottom View

4203539-3/G   04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No-Lead) package configuration.
    ⟨D⟩ The package thermal pad must be soldered to the board for thermal and mechanical performance.
    ⟨E⟩ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
          The Pin 1 identifiers are either a molded, marked, or metal feature.
   F. Package complies to JEDEC MO-241 variation BB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.
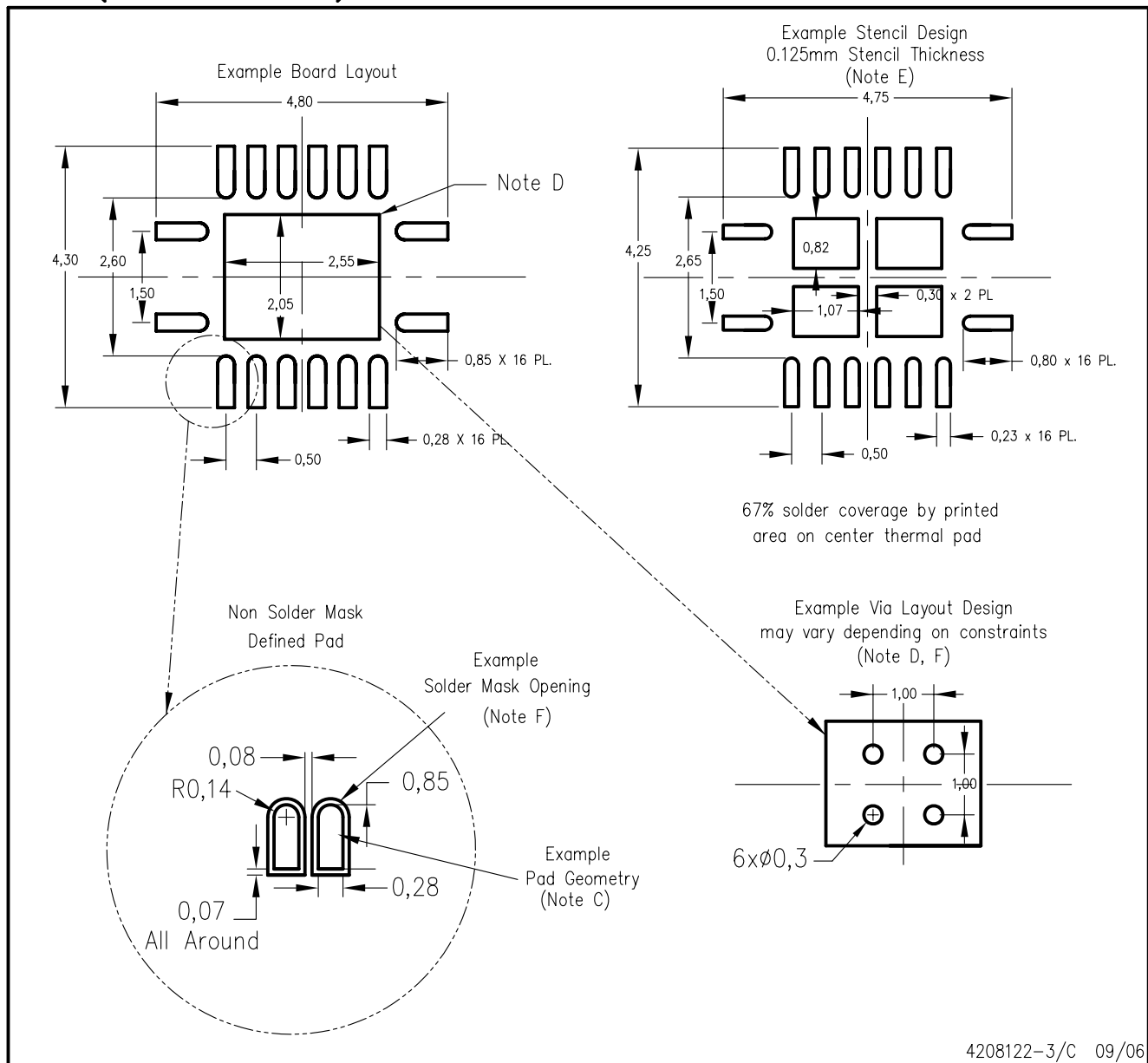
The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View
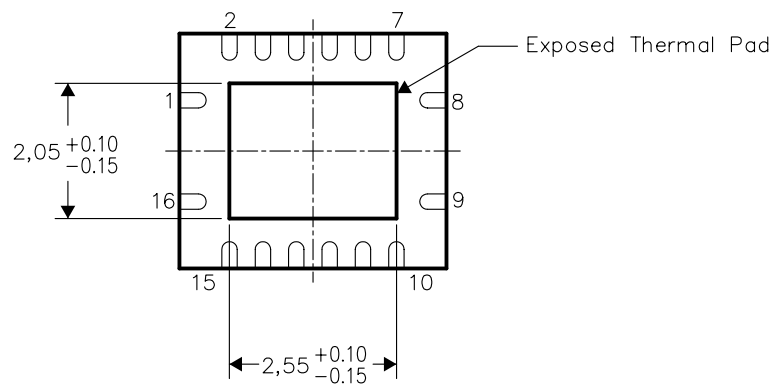
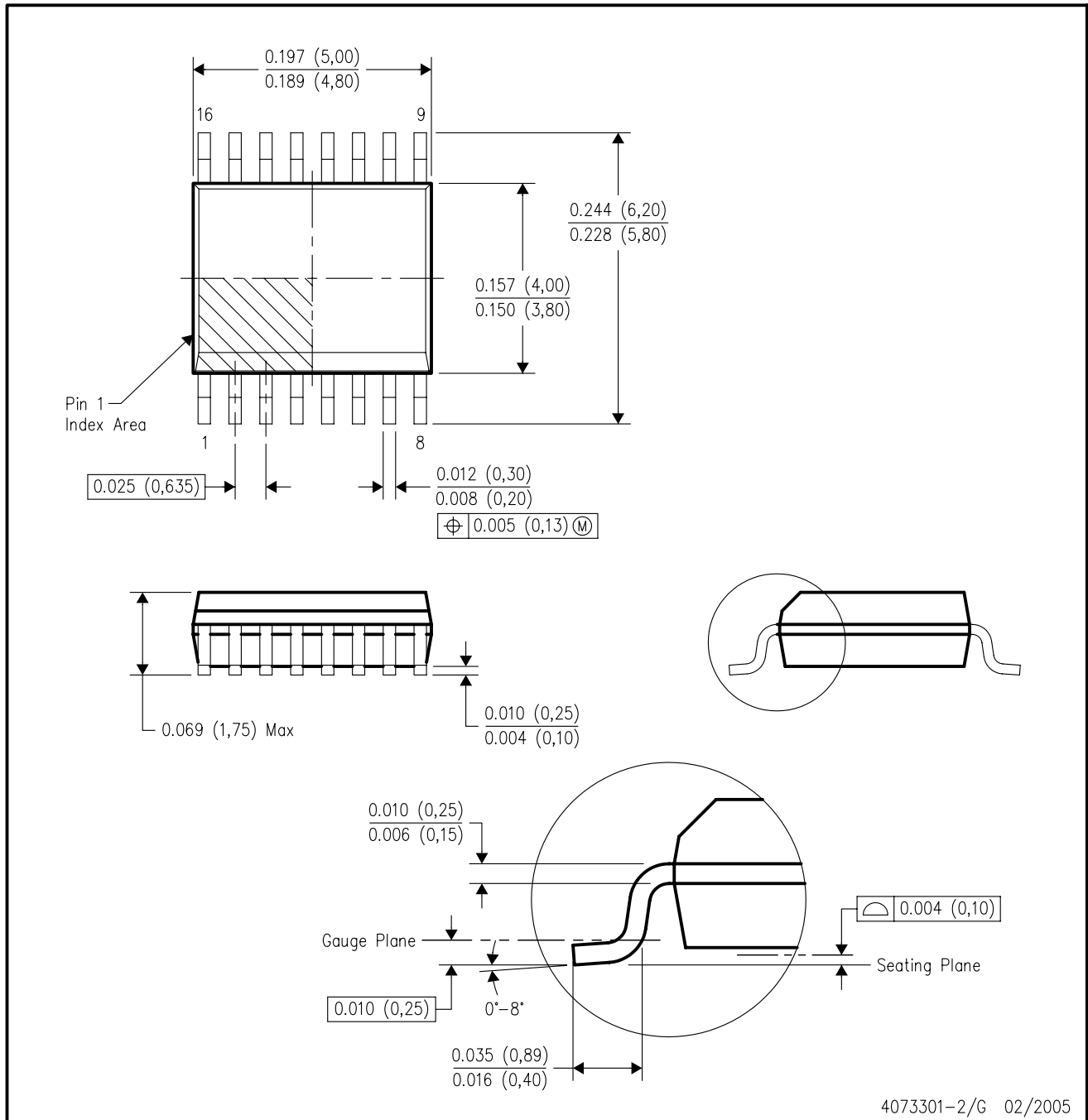NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R–PQFP–N16)

Example Board Layout

4,80

Note D

4,30   2,60

2,55

1,50

2,05

0,85 X 16 PL.

0,28 X 16 PL.

0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75

4,25   2,65

0,82

1,50

0,30 x 2 PL

1,07

0,80 x 16 PL.

0,23 x 16 PL.

0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14   0,85

Example
Pad Geometry
(Note C)

0,07   0,28

All Around

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6x⌀0,3

4208122–3/C   09/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Application Note, Quad Flat–Pack
              Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.   These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.   Customers should
              contact their board assembly site for stencil design recommendations.   Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DBQ (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   8

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.006 (0,15)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

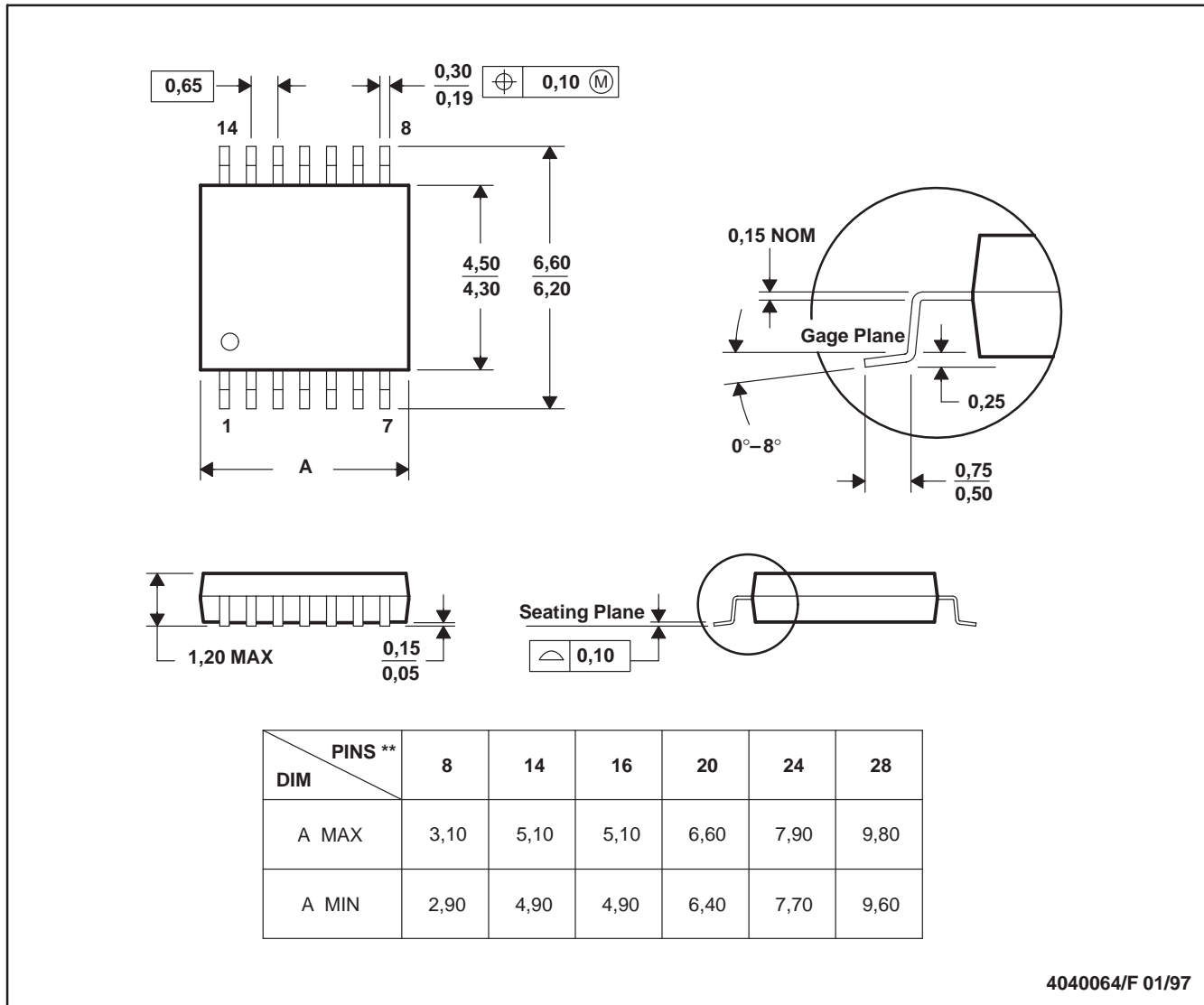4073301−2/G   02/2005

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D.   Falls within JEDEC MO−137 variation AB.

TEXAS
INSTRUMENTS
www.ti.com

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

0,65

0,30 / 0,19

⊕ 0,10 Ⓜ

14 8

4,50 / 4,30

6,60 / 6,20

1 7

A

0,15 NOM

Gage Plane

0°–8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address:　　Texas Instruments

　　　　　　　　　　Post Office Box 655303 Dallas, Texas 75265